FEATURES

Input voltage range: 3.6V ~20V

Output voltage is adjustable: 0.6V ~ 5.5V

Output current: two 2.5A or one 5A

Voltage adjustment ratio: 0.1% (typical value)

Load adjustment ratio: 0.2% (typical)

Multi-phase parallel current flow

External frequency synchronization function

Current mode control, fast transient response

PGOOD function

Adopt advanced packaging process

Optional CCM mode and BURST mode

Soft start/output voltage tracking

Overcurrent protection, short circuit protection, overheating protection

BGA packaging 6.25mm×6.25mm×2.42mm,

LGA packaging 6.25mm×6.25mm×1.82mm

APPLITIONS

Power supply for FPGA and DSP

Multi-voltage rail applications

DESCRIPTION

The LTM4622CN is a dual-channel DC/DC converter with 2.5A outputs and wide voltage input,available in both LGA and BGA packages.The package contains integrated switching controllers, power FETs, inductors, and all supporting components.It operates within a 3.6V to 20V input range and delivers 0.6V~5.5V output voltages (each set by individual external resistors).External implementation requires only large-capacity capacitors at theinput and output terminals (ceramic capacitors arerecommended based on ripple requirements).

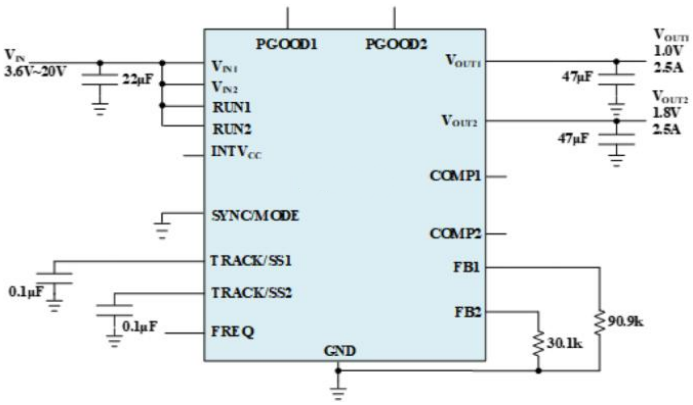
LTM4622CN can provide stable power voltage for FPGA, DSP and other digital circuits. When used in parallel with two paths,it can continuously provide up to 5A (2-phase) output current.

As a surface-mounted module, LTM4622CN is assembled on the PCB board by reflow soldering.The circuit has the characteristics of small size, high integration and light weight.

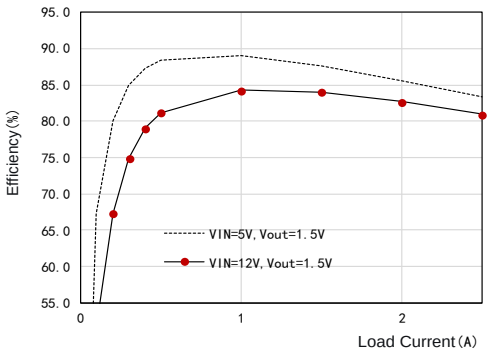
TYPICAL APPLITIONS

Typical Application Circuit for Dual-Channel Independent Operation Mode

(Double path 2.5A,1.0V,1.8V)



1.5V output load efficiency curve



ORDER INFORMATION

Device specifications	Package Type	Terminal Material	Product Marking	Moisture sensitivity level	temperature range (T_C)
LTM4622CN	25-LGA	Ni-Pd-Au	LTM4622CN	3	-40℃ ~ 125℃
	25-BGA	SAC305	LTM4622CN	3	-40℃ ~ 125℃

NOTES：For plastic encapsulated modules, it is recommended to bake at 125°C for 48 hours prior to use.

Product Operating Conditions

Absolute maximum rating of the circuit (note 1):

V_{IN1}, V_{IN2}..... -0.3V ~ 22V

V_{OUT} ..... -0.3V ~ 6V

PGOOD1, PGOOD2 ..... -0.3V ~ 18V

RUN1, RUN2 .....-0.3V ~ VIN+0.3V

$INTV_{CC}$ ..... -0.3V ~ 3.6V

TRACK/SS1, TRACK/SS2 ..... -0.3V ~ 3.6V

SYNC/MODE ..... -0.3V ~ 3.6V

FB1, FB2 .....-0.3V ~ INTVCC

COMP1, COMP2..... -0.3V ~ 3.6V

Output current range:

I_{OUT}= 0 ~ 3A: single channel independent operation

I_{OUT}=N×(0 ~ 3A): N is the number of parallel channels

Lead soldering temperature: 250℃ (30s)

Storage temperature range (T_{stg}): -55℃ ~ 125℃

Recommended operating conditions for this circuit:

Input voltage range V_{IN} ..... 3.6V ~ 20V

Output voltage range V_{OUT}.....0.6V ~ 5.5V

Output current range:

I_{OUT}= 0 ~ 2.5A :single channel independent operation

I_{OUT}=N×(0 ~ 2.5A): N is the number of parallel channels

Working shell temperature TC:-40℃ ~ 125℃

Recommended temperature curve for board welding:

Typical lead curve (peak temperature: 210℃~230℃, liquefaction time: 30s~90s);

Typical lead-free curve (peak temperature: 240℃ ~245℃, liquefaction time: 30s~90s);

Note 1: Stress above the values listed in the "absolute maximum rating" section may cause permanent damage to the device. Excessive operation under any absolute maximum conditions may affect the reliability and service life of the device.

Thermal Resistance Of The Product

Test conditions: The product is soldered on a test board with dimensions 130mm×130mm×1.6mm. The four-layer board features large copper plating on both surface and inner layers, with a thickness of 1oz. As thermal resistance parameters are closely related to actual application environments, measurement results may vary depending on different conditions. This parameter is provided for reference only.

product model	package type	product size (mm^3)	Test board size (mm^2)	Chip to environment Thermal resistance to temperature θ_{JA}	Chip to substrate Thermal resistance to temperature $\theta_{JCbottom}$	Chip to top Thermal resistance to temperature θ_{JCtop}
LTM4622CN	LGA	6.25×6.25×1.82	≥130×130 (four layers)	19℃/W	9℃/W	15℃/W
	BGA	6.25×6.25×2.42	≥130×130 (four layers)	19℃/W	9.5℃/W	15℃/W

Product Electrical Characteristics

Indicates that-40℃ ≤ T_C ≤ 125℃. Unless otherwise stated, the test conditions are all T_A = 25℃.

Symbol	Parameter	Test conditions (note 2)		Limit			Unit
				Min	Typ	Max	
V_{IN}	input voltage	—	●	3.6	—	20.0	V
$V_{IN-3.3}$	3.3V input voltage	V_{IN} = $INTV_{CC}$		3.1	3.3	3.5	V
$V_{OUT(RANGE)}$	Output voltage range	—	●	0.6	—	5.5	V
$V_{OUT(DC)}$	output voltage	C_{IN}=22μF，C_{OUT}=47μF ceramic×2，MODE =GND，V_{IN}=3.6V~20V，R_{FB}=40.2kΩ，I_{OUT}= 0～2.5A (note 3)	●	1.477	1.500	1.523	V
input characteristics							
$I_{Q(VIN)}$	Input power supply bias current	V_{IN}=12V，V_{OUT}=1.5V，MODE =$INTV_{CC}$		—	500	—	μA
		V_{IN}=12V，V_{OUT}=1.5V，MODE =GND	●	—	15	—	mA
		Stop, RUN1=RUN2=0	●	—	45	—	μA
$I_{S(VIN)}$	Input power current	V_{IN}=12V，V_{OUT}=1.5V，I_{OUT}= 2.5A	●	—	0.39	—	A
output characteristic							
$I_{OUT(DC)}$	output	V_{IN}=12V，V_{OUT}=1.5V (Note 3)		0	—	2.5	A
S_V	voltage regulation	V_{OUT}=1.5V，I_{OUT}=0A，V_{IN}=3.6V~20V	●	—	0.1	1.5	%
S_I	load regulation	V_{OUT}=1.5V，I_{LOAD}=0A~2.5A	●	—	0.2	1.0	%
V_{PP}	Output ripple voltage	I_{OUT}=0A, C_{OUT}=47μF ceramic×2, V_{IN}=12V，V_{OUT}=1.5V	●	—	10	20	mV
F_{OSC}	switching frequency	—		0.8	1.0	1.2	MHz
$\triangle V_{OUT(START)}$	Start overshot	C_{OUT}=47μF ceramic ×2, V_{IN}=12V，V_{OUT}=1.5V，I_{OUT}=0A		—	30	50	mV
t_{START}	start time	C_{OUT}=47μF ceramic × 2, no load, TRASK/SS=0.01μF，V_{IN}=12V，V_{OUT}=1.5V		—	4.3	5.0	ms
$\triangle V_{OUTLS}$	Dynamic step overshoot	Load: 0%~50%~0%, COUT=47μF ceramic ×2, V_{IN}=12V，V_{OUT}=1.5V		—	120	170	mV
t_{SETTLE}	Dynamic recovery time	Load: 0%~50%~0%, C_{OUT}=47μF ceramic×2,V_{IN}=12V,V_{OUT}=1.5V		—	25	45	μs
I_{OUTPK}	Output flow limit point	V_{IN}=12V，V_{OUT}=1.5V		3	4	—	A
control section							
V_{FB}	FB pin voltage	V_{IN}=12V，V_{OUT}=1.5V，I_{OUT}=0A		0.592	0.600	0.608	V
V_{RUN}	RUN enable threshold	V_{RUN} rising edge		1.15	1.27	1.35	V
		V_{RUN} trailing edge		0.97	1.00	1.03	
PGOOD	PGOOD Flip-flop threshold	V_{FB} slope up (negative)		-14	-8	—	%
		V_{FB} slope up (positive)		—	8	14	%

Note 2: The electrical characteristics index test is based on laboratory conditions and the module is welded to the evaluation board for testing.

Note 3: See the output current derating curves for different $V_{IN,}$ V_{OUT} and T_A conditions.

Note 4: See the output current reduction curve for different V_{IN}, V_{OUT}, and T_A conditions.

PIN CONFIGURATION

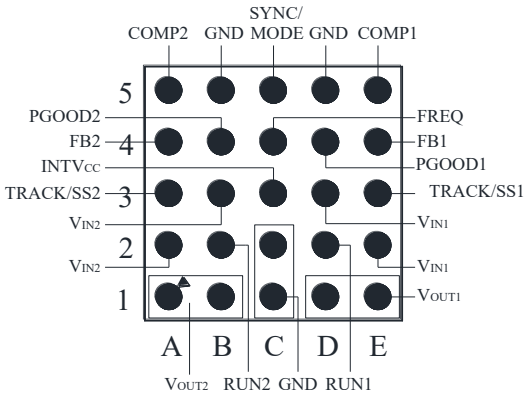


Figure 1 Top view of pin definition

Pin	Pin definitions	Pin description
D3，E2	VIN1	Power input pins on each channel. Apply the input voltage between these pins and the GND pin. It is recommended to place the input decoupling capacitors directly between each input and ground.
A2，B3	VIN2	
D1，E1	VOUT1	Power output pins of each channel. Apply output load between these pins and GND pins. It is recommended to directly place the output decoupling capacitor between each output and ground.
A1，B1	VOUT2	
C1，C2，B5，D5	GND	Input and output loop power is provided for each circuit. Large PCB copper area is used to connect all GND together.
D4	PGOOD1	Each channel displays the normal drain open indicator. When the voltage on the FB pin is outside ±8% of the internal 0.6V reference, PGOOD is pulled to ground.
B4	PGOOD2	
C3	INTVCC	The 3.3V regulator output terminal inside each channel is powered by this voltage to control the circuit and internal power driver.
E3	TRACK/SS1	The output voltage tracking and soft-start input pin controls the rising time of the output voltage. When this pin is applied with a voltage below 0.6V, the FB pin tracks the TRACK voltage. When the pin voltage exceeds 0.6V, the tracking function ceases and the internal reference resumes control of the error amplifier. This pin features a 1.4μA internal pull-up current, so installing a capacitor between this pin and ground provides soft-start functionality.
A3	TRACK/SS2	
C5	SYNC/MODE	The external synchronization signal input and channel mode selection pins. Connecting this pin to ground activates forced continuous operation mode. When connected to INTVCC, the module operates in an efficient burst mode under light load conditions. Applying a clock signal to this pin automatically locks into forced continuous operation mode.
D2	RUN1	Enable pin: Do not leave this pin empty during normal use.
B2	RUN2	
E4	FB1	The inverting input terminal of the error amplifier in each channel. Within the module, a 60.4kΩ resistor is connected between this pin and VOUT. Different output voltages can be configured by externally connecting resistors between the FB terminal and GND. When operating in parallel, all modules' FB terminals must be connected together.
A4	FB2	
E5	COMP1	The current control threshold setting for each channel and the compensation terminal of the error amplifier. The threshold of the current comparator increases as the control voltage increases. When used in parallel, connect this pin together.
A5	COMP2	
C4	FREQ	Frequency setting pin. The internal frequency is default 1MHz. A resistor between this pin and GND can increase the frequency, and a resistor

Pin	Pin definitions	Pin description
		added between this pin and INTVCC can reduce the frequency.

Product Block Diagram

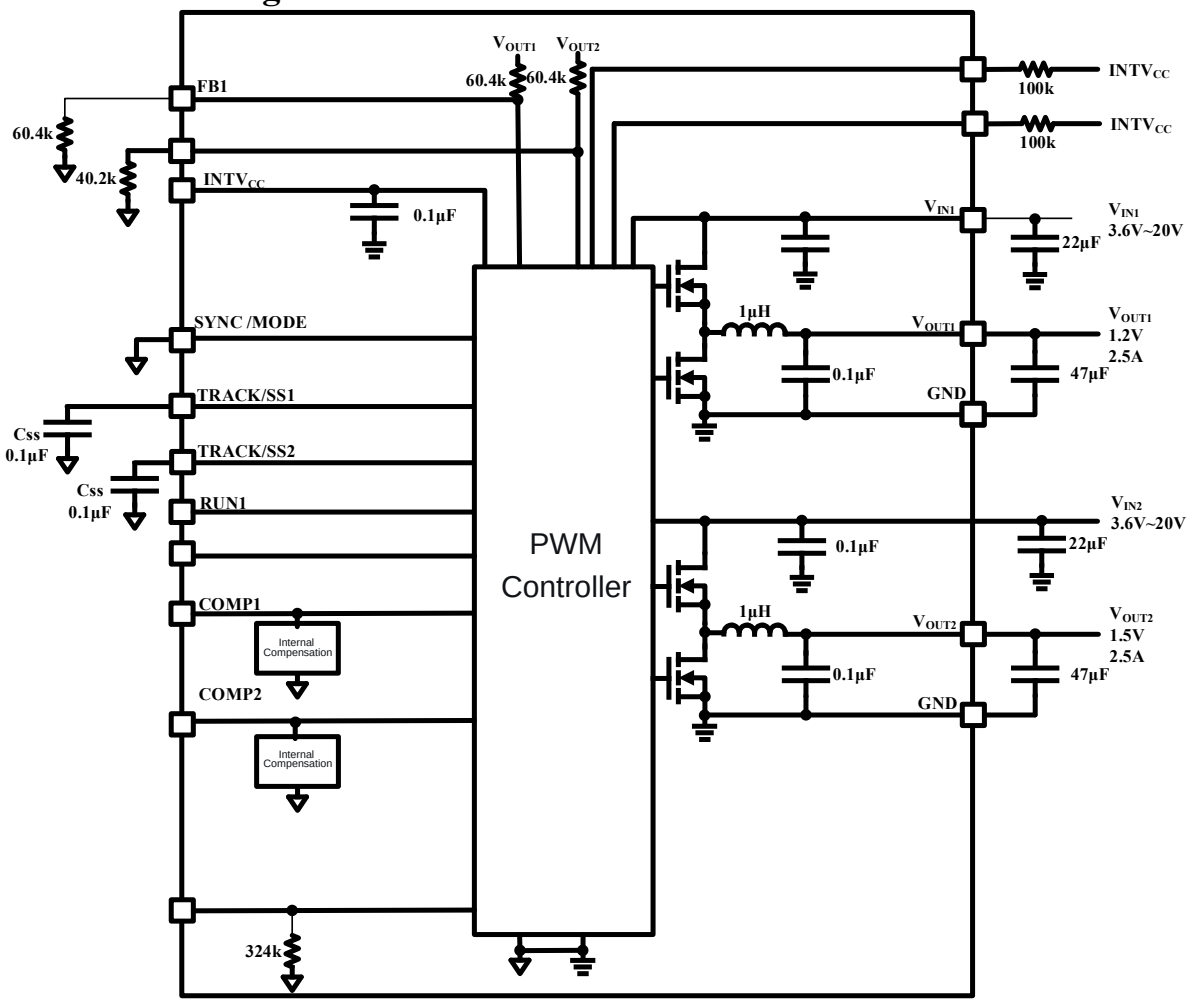


Figure 2 LTM4622CN principle block diagram

Product typical performance

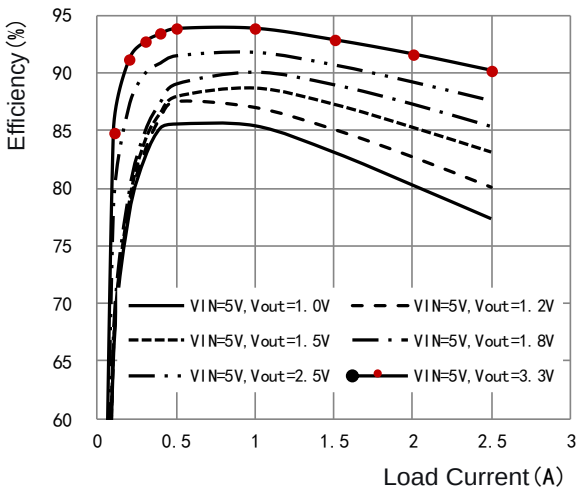


Figure 3 5V input-load-efficiency curve

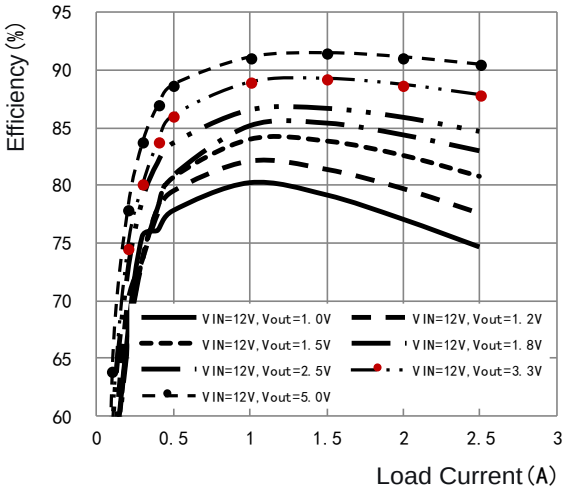
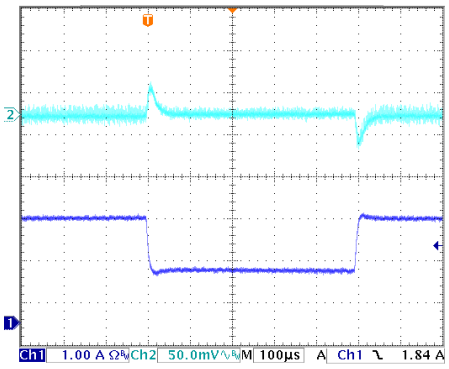


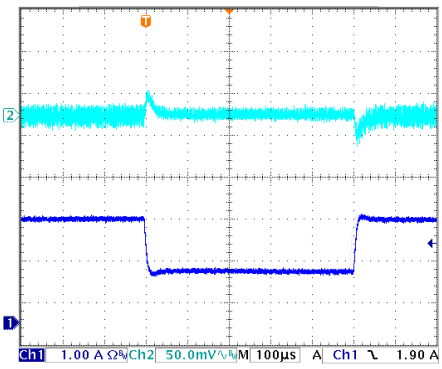
Figure 4 12V input-load-efficiency curve



V_{IN}=12V, V_{OUT}=1.5V, I_{OUT}=1.25A~2.5A~1.25A,

f_{SW}=1kHz, C_{OUT}=47µF (ceramic) × 2

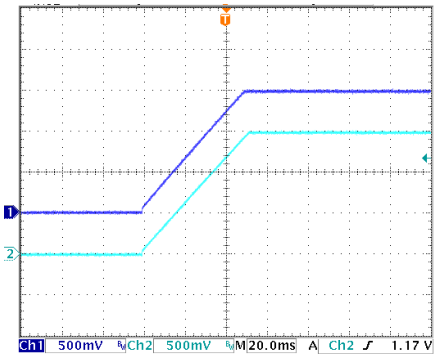
Figure 5 Load-dynamic curve



V_{IN}=12V, V_{OUT}=1.0V, I_{OUT}=1.25A~2.5A~1.25A,

f_{SW}=1kHz, C_{OUT}=47µF (ceramic)×2

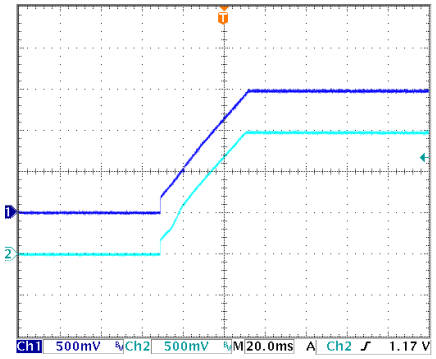
Figure 6 Load-dynamic curve



V_{IN}=12V, V_{OUT}=1.5V, I_{OUT} =0A,

C_{OUT}=47µF (ceramic) × 2, C_{SS}=0.1µF

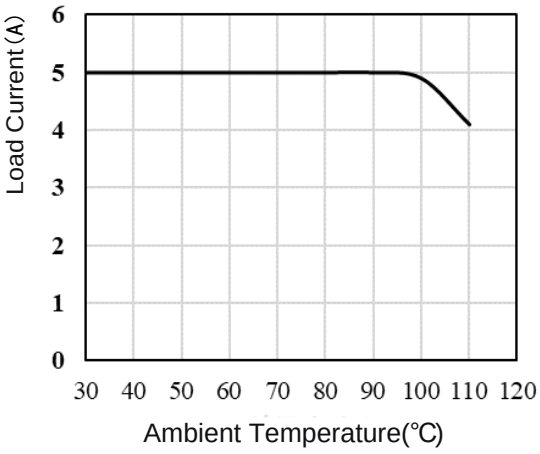
Figure 7 Startup waveform



V_{IN}=12V, V_{OUT}=1.5V, I_{OUT} =2.5A,

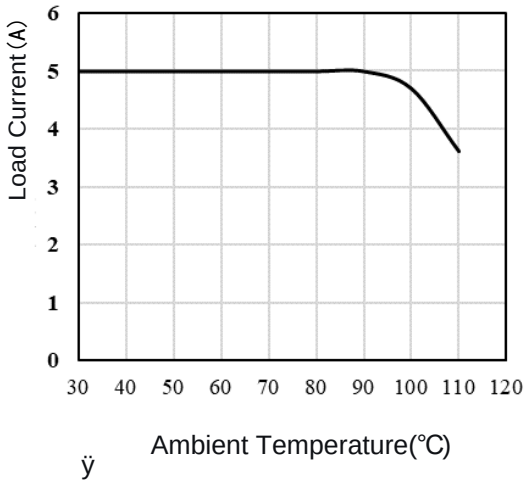
C_{OUT}=47µF (ceramic) × 2, C_{SS}=0.1µF

Figure 8 Startup waveform



VI_N=5V,V_{OUT}=1.0V, T_C ≤125℃, dual parallel, closed environment

Figure 9 Reddown curve



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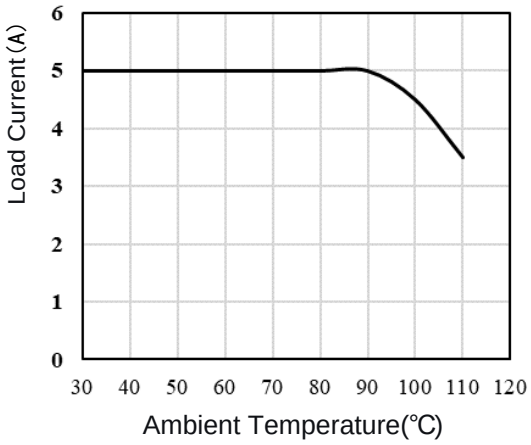
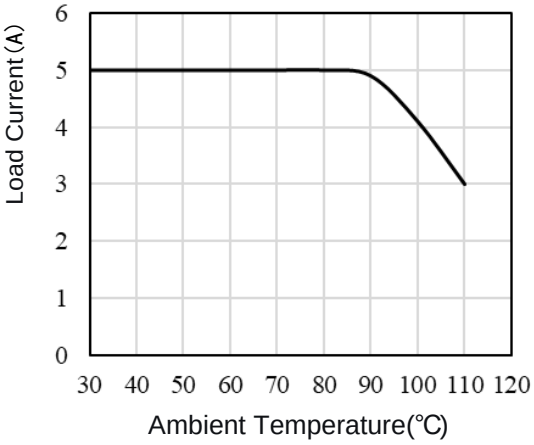
V_{IN}=12V,V_{OUT}=1.0V,T_C ≤ 125℃, dual parallel, closed environment

Figure 10 Reddown curve



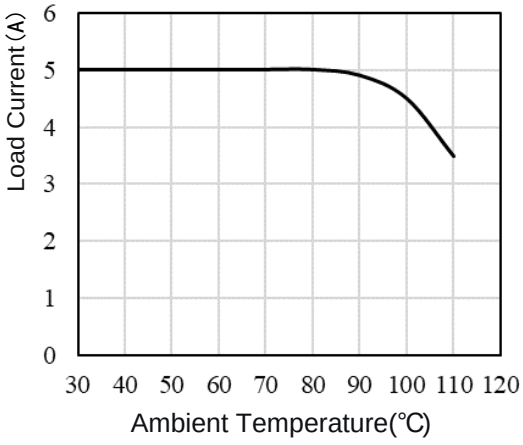
V_{IN}=5V,V_{OUT}=1.5V, T_C ≤ 125℃, dual parallel, closed environment

Figure 11 Reddown curve



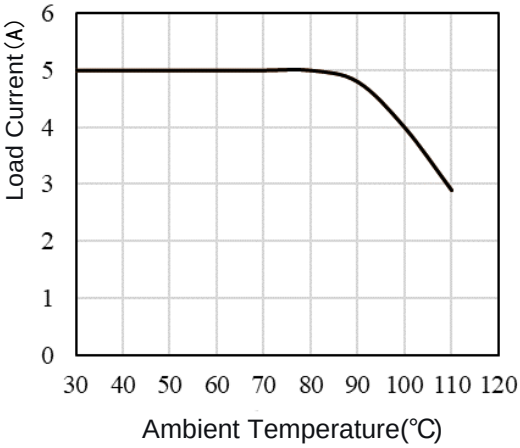
V_{IN}=12V,V_{OUT}=1.5V,T_C ≤ 125℃, dual parallel, closed environment

Figure 12 Reddown curve



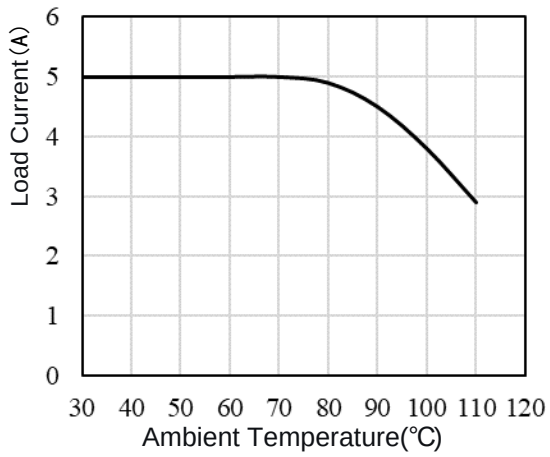
V_{IN}=5V,V_{OUT}=2.5V, T_C ≤ 125℃, dual parallel, closed environment

Figure 13 Reddown curve



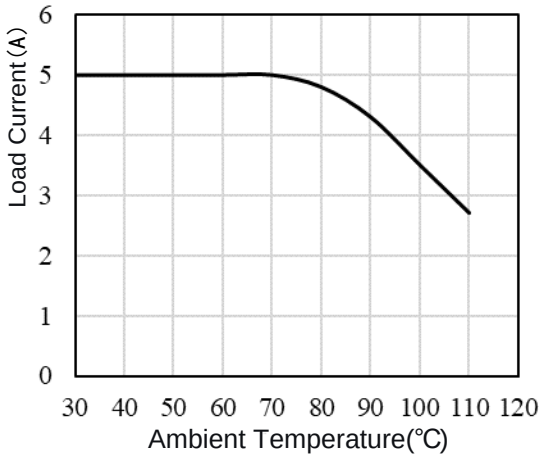
V_{IN}=12V,V_{OUT}=2.5V, T_C ≤125℃, dual parallel, closed environment

Figure 14 Reddown curve



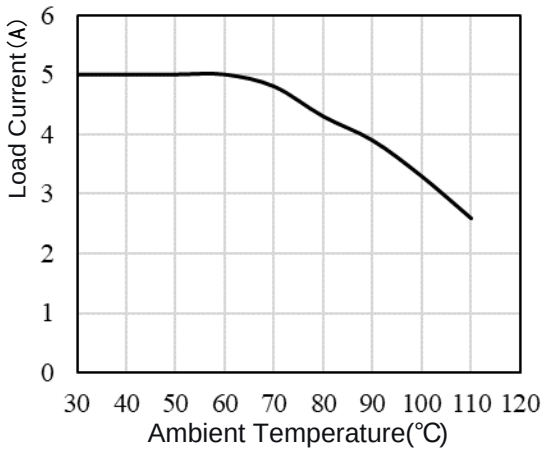
V_{IN}=5V,V_{OUT}=3.3V, T_C ≤ 125℃, dual parallel, closed environment

Figure 15 Reddown curve



V_{IN}=12V,V_{OUT}=3.3V, T_C ≤125℃, dual parallel, closed environment

Figure 16 Reddown curve



V_{IN}=12V, V_{OUT}=5V, T_C≤125℃, dual parallel, closed environment

Figure 17 Reddown curve

Application Note

V_{IN} to V_{OUT} voltage reduction ratio

The maximum duty cycle of each channel is limited by the minimum turn-off time, and the minimum duty cycle is limited by the minimum turn-on time.

Minimum turn-off time limits maximum duty cycle, which can be calculated by the following formula:

$$D_{MAX} = 1 - t_{OFF(MIN)} \times f_{SW}$$

In this formula, OFF (MIN) is the minimum turn-off time (typically 45ns for LTM4622CN), and fSW is the switching frequency. In contrast, the minimum conduction time limit restricts the minimum duty cycle, which can be calculated by the following formula:

$$D_{MIN} = t_{ON(MIN)} \times f_{SW}$$

The $t_{ON\ (MIN)}$ in the formula represents the minimum conduction time (typically 20ns for the LTM4622CN). When the actual duty cycle of the product falls below this minimum threshold, the output voltage remains adjustable but with reduced switching frequency. For additional thermal derating design considerations, refer to the derating curves in Figures 9-17 of this product manual.

Output voltage

The PWM controller has a reference voltage of 0.6V. As shown in the "Principle Block Diagram", each channel's VOUT pin and FB pin of the voltage regulator are connected to an internal feedback resistor with a 60.4kΩ value. By adding a resistor RFB between the FB pin and GND, the output voltage can be configured as follows:

$$R_{FB} = \frac{0.6V}{V_{OUT} - 0.6V} \times 60.4k$$

Table 1 Correspondence between output voltage and resistance value of RFB resistor

V_{OUT}(V)	0.6	1.0	1.2	1.5	1.8	2.5	3.3	5.0
R_{FB} (kΩ)	Open Circuit	90.9	60.4	40.2	30.1	19.1	13.3	8.25

Note that when the output voltage range is 2.5V ~5.5V, the switching frequency should be increased. Please see the working frequency chapter.

For the case of N channels working in parallel, RFB can be solved by the following formula:

$$R_{FB} = \frac{0.6V}{V_{OUT} - 0.6V} \times \frac{60.4k}{N}$$

Input decoupling capacitor

The LTM4622CN should be connected to a low AC impedance DC power supply. For each channel of the voltage regulator, it is recommended to use a 22μF ceramic input capacitor to achieve RMS ripple curren decoupling.

When the input power lin is long, there are inductive parasitic parameters, or the capacitance is insufficient, a large capacity input capacitor can be placed. This large capacity capacitor can be a tantalum capacitor.

If inductor current ripple is not considered, the RMS current of the input capacitor can be estimated using the following formula:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\ \%} \times \sqrt{D \times (1 - D)}$$

The η % in this formula is the estimated efficiency of the power module.

Output decoupling capacitors

Through an optimized high-frequency, high-band width design, each channel of the voltage regulator requires only one 47μF ceramic output capacitor to achieve low-voltage ripple and excellent transient response. To ensure effective filtering and operational stability across three temperature ranges, it is generally recommended that each channel's output

filter capacitor should not be less than 47μF. System designers can configure output filter capacitors according to practical application requirements. For enhanced high-frequency noise filtering, additional capacitors with capacities such as 1μF, 0.1μF, or 1000pF may be configured.

The output filter capacitor should be fully connected to the output power circuit,as shown in the PCB layout, to ensure good filtering effect.During layout,multipl vias can be arranged to realize the interconnection of multi-layer power supply.

Burst mode

In applications requiring high efficiency under moderat e current conditions,the Burst Mode(BURST) should be employed by connecting the SYNC/MODE pin to INTVCC. During BURST operation,the Current Inverting comparator (IREV) detects negative inductive current and turns off the bottom power MOSFET, enabling discontinuous operation and improved efficiency. If both power MOSFETs remain off, the output capacitor will supply load current until the COMP voltage rises above zero-current level, thereby initiating another cycle.

Forced continuous conduction mode

For applications requiring fixed-frequency operation with minimal output ripple, the forced continuous conduction mode should be employed.To activate this mode, connect the MODE pin to ground. In this configuration, inductor current is allowed to flow in reverse, the COMP voltage controls the current comparator's threshold, while the MOSFET switch remains active during each oscillator pulse cycle.

Service frequency

The LTM4622CN's operating frequency is optimized to deliver high efficiency while maintaining a compact package size and minimal output ripple voltage.The defaul operating frequency is set internally at 1MHz, requiring no additional frequency adjustment in most applications.

If any operating frequency other than 1MHz is required in the application, the operating frequency can be in creased by adding a resistor RFSET between the FRE QUENTION pin and SGND.The operating frequency can be calculated as:

$$f\ (Hz) = \frac{3.2e11}{324k \| R_{FSET}(\Omega)}$$

To reduce switching current ripple,an output of 2.5V to 5.5V requires a working frequency of 1.5MHz to 2.5MHz.

Table 2 Correspondence between output voltage, fSW and RFSET resistance value

output voltage	0.6V~1.8V	2.5V	3.3V	5V
fSW	1MHz	1.5MHz	2MHz	2.5MHz
RFSET	Open	649kΩ	324kΩ	215kΩ

The operating frequency can also be reduced by adding a resistor between the FREQ pin and INTVCC. The calculation method is:

$$f\ (Hz) = 1MHz - \frac{5.67e11}{R_{FSET}(\Omega)}$$

Programmable operating frequency range is 800kHz to 4 MHz.

Frequency synchronism

The power module incorporates a phase-locked loop (PLL) comprising an internal voltage-controlled oscillator and a phase detector. This configuration enables all internal MOSFET switches to be synchronized with the rising edge of a single external clock, which must operate within ±30% of ±1MHz. A pulse detection circuit monitors clock signals from the CLKIN pin to activate the PLL, requiring these pulses to maintain a minimum duration of 100ns.

The clock high must be above 2V and the clock low must be below 0.3V.

Multiple channels work in parallel

For loads requiring an output current of more than 2.5A,multiple voltage regulator channels of the LTM4622CN can be connected in parallel to provide a greater output current without increasing input and output voltage ripple.

Multi-phase parallel connection significantly reduces ripple current levels in both input and output capacitors.The reduction ratio of RMS input ripple current to effective ripple frequency is determined by the number of phases used (assuming the input voltage exceeds the product of the number of phases and outpu voltage).When all output are interconnected to achieve a single high-current design, the decrease in output ripple amplitude also correlates with the number of phases utilized.

The LTM4622CN is a current-mode control module with excellent current balancing characteristics when used in parallel. This balances heat on each channel. When used in parallel, connect the RUN,TRACK/SS, FB, and COMP pins of each channel together.

Soft start and output voltage tracking

Each channel's TRACK/SS pin enables both soft-start functionality and output voltage tracking. By connecting a capacitor to ground through the TRACK/SS pin, users can configure the output voltage ramp-up time. An internal 1.4μA current source charges the external soft-start capacitor to near the INTVCC voltage level. When the TRACK/SS voltage drops below 0.6V, it automatically switches to the internal 0.6V reference voltage to regulate the output. The total soft-start duration can be calculated using the following formula:

$$tss = 0.6 \times \frac{C_{SS}}{1.4\,\mu A}$$

The CSS in the schematic refers to the capacitors on the TRACK/SS pins. When TRACK/SS is left floating,the LTM4622CN features an internal 400μs soft-start time.

PGOOD function

The PGOOD pin is an open-drain pin designed to monitor output voltage stability. This pin tracks voltage fluctuations within ±8% of the set threshold. As it cannot directly output high signals, a pull-up resistor (typically 4.7kΩ– 100kΩ) is recommended for connection to the INTVCC pin. To prevent PGOOD failures during transient or dynamic VOUT variations, the LTM4622CN incorporates a 40μs fade-out delay at its PGOOD falling edge.

Stability compensation

The LTM4622CN module's internal compensation loop for each voltage regulator is specifically designed and optimized for applications requiring onl low ESR ceramic output capacitors. In scenarios where high-capacity output capacitors are needed to reduce output ripple and dynamic transient spikes, a 10pF to 100pF capacitor (CFF) should be added between the VOUT and FB pins to enhance phase margin.

Enablement function

The RUN pin serves as a power-on enable.It controls the activation of each channel's switching mode in the LTM4622CN.When any enable pin is pulled low, the LTM4622CN enters shutdown mode. The power transistor can only be activated when the enable pins are set to a 1.2V or higher level.

Overtemperature protection

The internal over temperature protection function circuit monitors the junction temperature of the module. If the junction temperature reaches about 160°C, the power switch will be cut off until the temperature drops by about 25°C.

Low input application

When the VIN pin is connected to the INTVCC pin, the LTM4622CN can operate on a 3.3V input voltage. The application circuit diagram is shown in Figure 25. Note that the maximum rated voltage of the INTVCC pin is 3.6V.

Recommended PCB layout

① Welding pad design

LG pad recommended size diameter 0.63mm, BGA pad recommended size diameter 0.63mm.

It is recommended to adjus th solder mask window design for large copper-clad power pin pads such as VIN,GND,and VOUT.Otherwise,PCB manufacturers may use the default 0.1mm window size in standard software, resulting in slightly larger pads that might mismatch with independent pin pads.Such dimensional discrepancies could cause solder compression or stretching on other pads during reflow soldering when modules are oriented perpendicular to the PCB board.

② PCB board layout

In order to optimize its electrical and thermal properties, the layout needs to be considered.

a、For high current paths, use large PCB copper foil areas, including VIN, GND, VOUT, to help reduce PCB conduction loss and thermal stress;

b. Place a high frequency ceramic capacitor near the VIN, GND and VOUT pins to reduce high frequency noise;

c. Place a dedicated power layer under the module;

d. In order to minimize the through-hole conduction loss and reduce the thermal stress of the module, multiple vias can be used to connect the top layer and other power layers;

e. do not layout the vias directly on the pads, unless the vias are filled;

f. For the parallel mode, the pins COMP, FB, RUN, and TRACK/SS are connected together. An internal layer is used to connect these pins together.

Figure 18 provides a recommended layout for the PCB board.

③ Recommended pads

The typical BG solder ball diameter of LTM4622CN B product is 0.76mm, and the lead size diameter of LTM4622CN L is 0.64mm. According to IPC-7351B surface mount component pad design specification, users are recommended to design the package library according to the dimensions in Table 3.

Table 3 Recommended LTM4622CN pad dimensions

product model	Package Type	BGA ball diameter (mm)	Recommended pad window size (mm)
LTM4622CN	25-LGA	0.76	Φ0.63
	25-BGA	——	Φ0.63

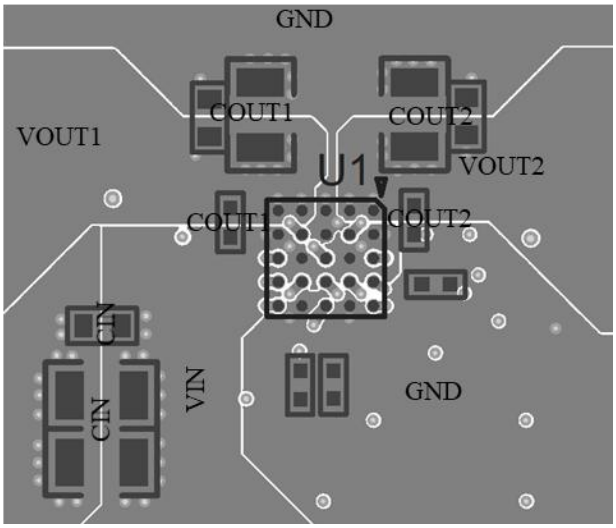


Figure 18 LTM4622CN recommended PCB layout

Product typical application (note 4, note 5, note 6)

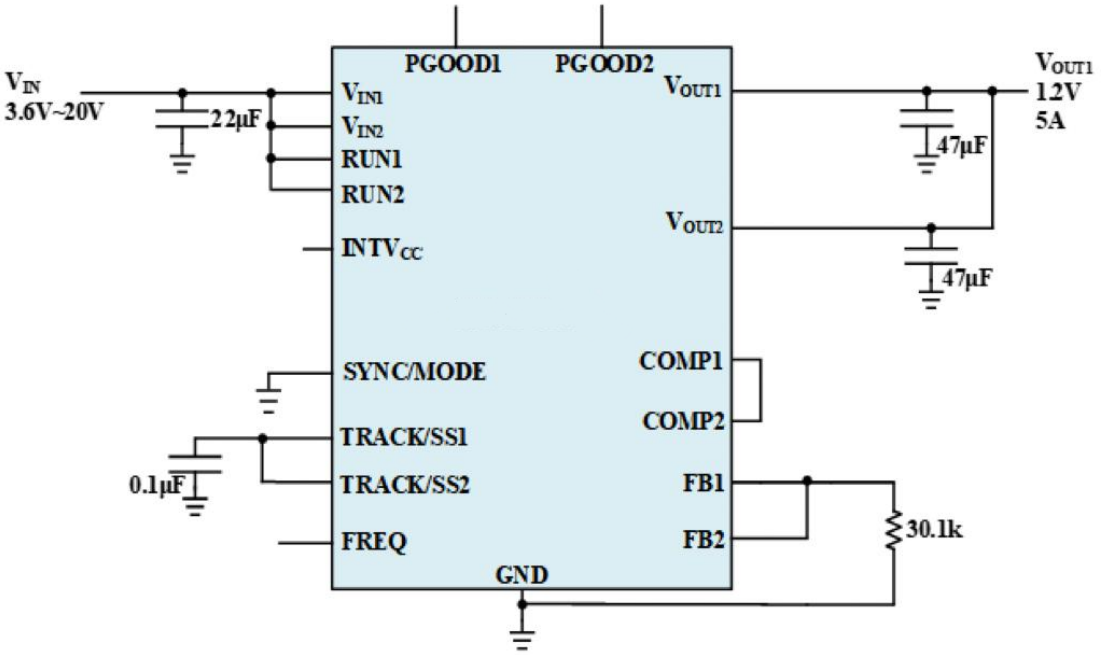


Figure 19 Dual parallel outputs 1.2V, load 5A

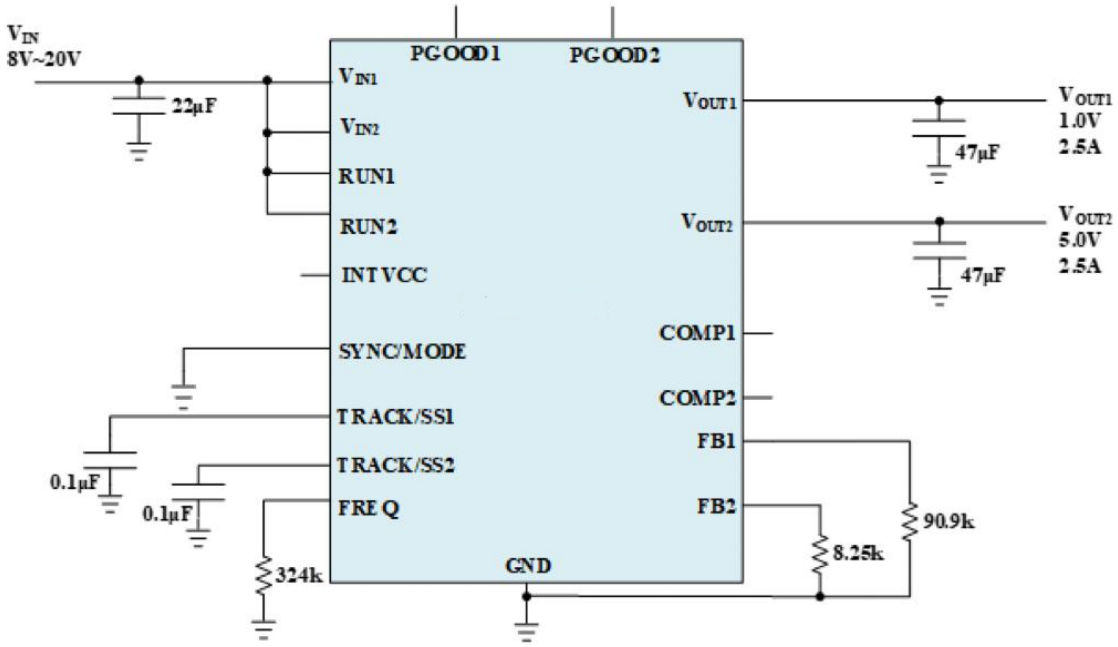


Figure 20 Single output 1.0V,5.0V, load 2.5A

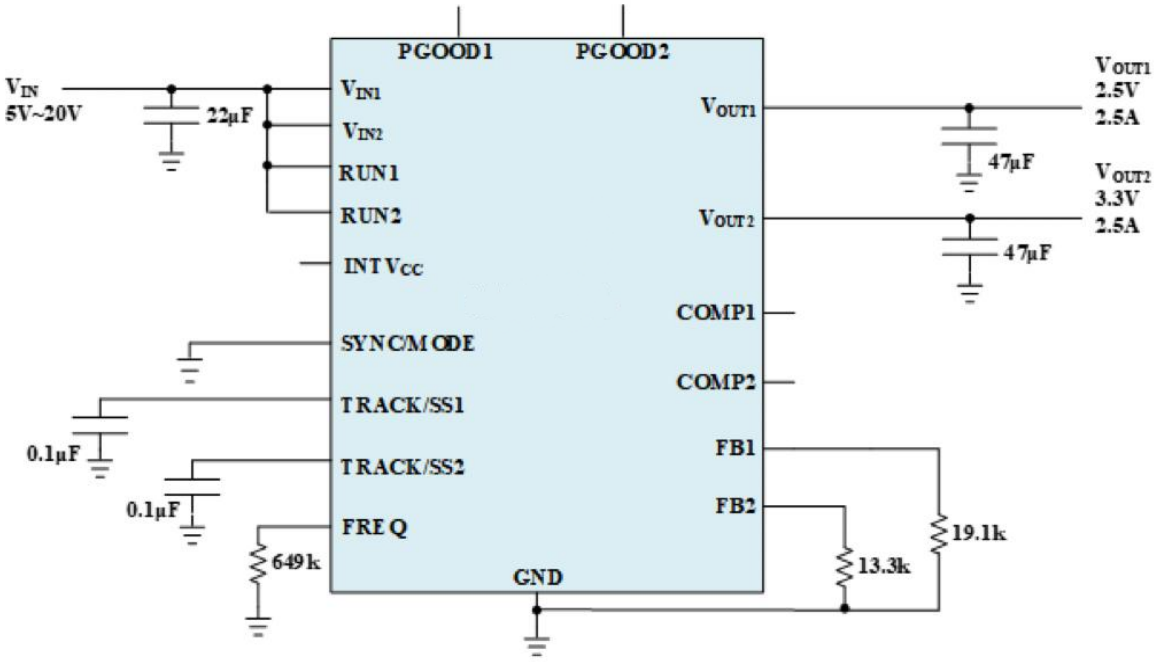


Figure 21 Single output 2.5V,3.3V, load 2.5A

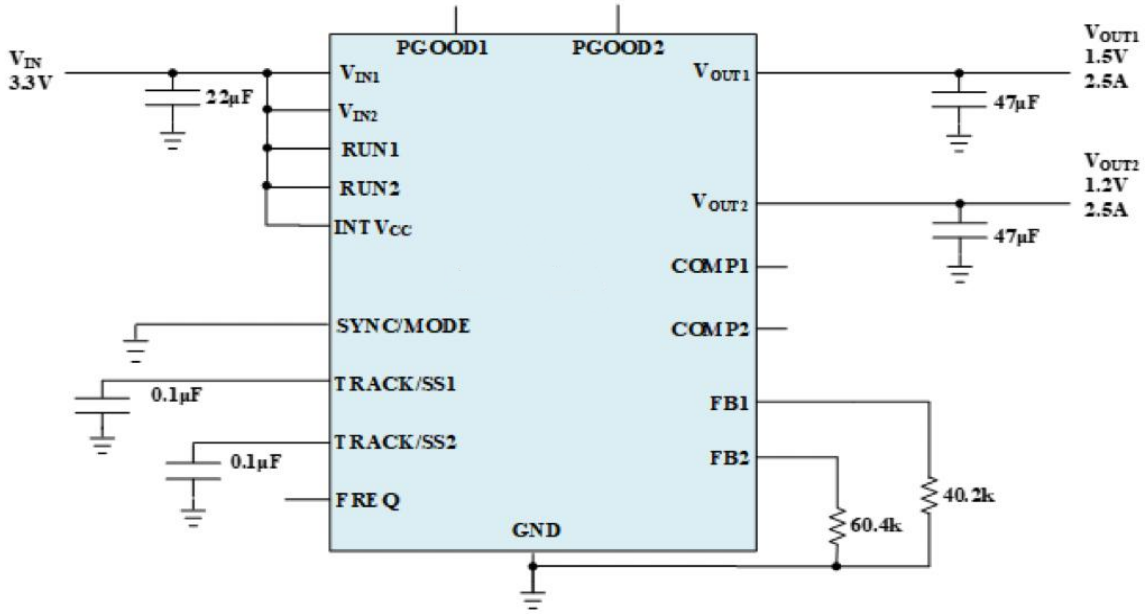


Figure 22 3.3V input voltage, single output 1.5V,1.2V, load 2.5A

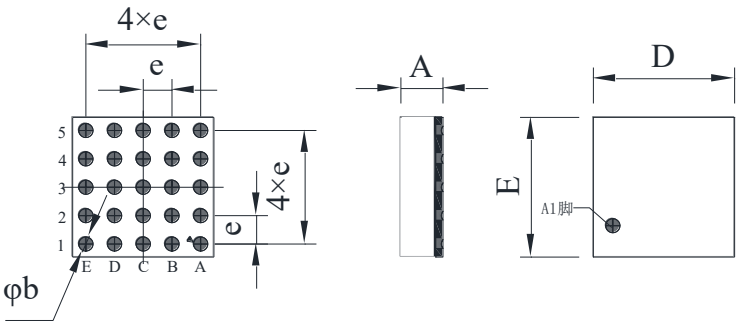
Note 4: The typical application circuit (including the one on page 1) is optimized for optimal module performance configuration and is suitable for most application scenarios. Users may make appropriate adjustments based on board space dimensions and output noise requirements during practical implementation.However, the input VIN-to-ground capacitance should not be less than 22μF, and the output capacitor should not be less than 47μF – values below these thresholds may compromise operational stability.

In addition to high-capacity capacitors, multiple 1μF or 0.1μF capacitors can be added to filter high-frequency noise.

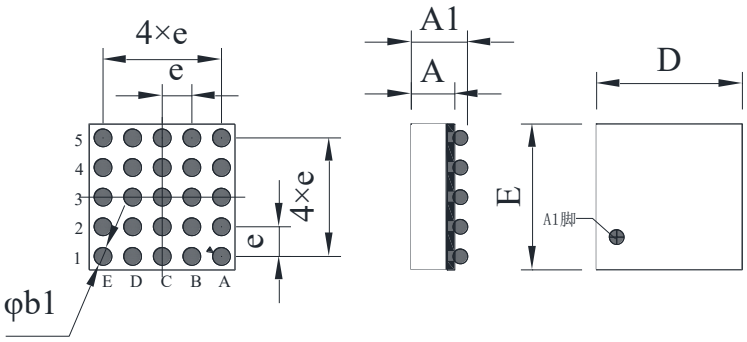
Note 5: In order to suppress the surge current during startup, it is not recommended to leave the TRACK/SS pin of each channel empty. A capacitor between 10nF and 220nF can be configured.

Note 6: The operating frequency can be reduced by adding a resistor between the FREQ pin and INTVCC.

Product Size



a) LTM4622CN(LGA)



b) LTM4622CN(BAG)

Size symbols	numeric value		
	minimum	nominal	maximum
A	1.72	1.82	1.92
A1	2.32	2.42	2.52
D	6.05	6.25	6.45
E	6.05	6.25	6.45
Φb	0.54	0.64	0.74
Φb1	0.66	0.76	0.86
e	——	1.27	——

Figure 23 External dimensions

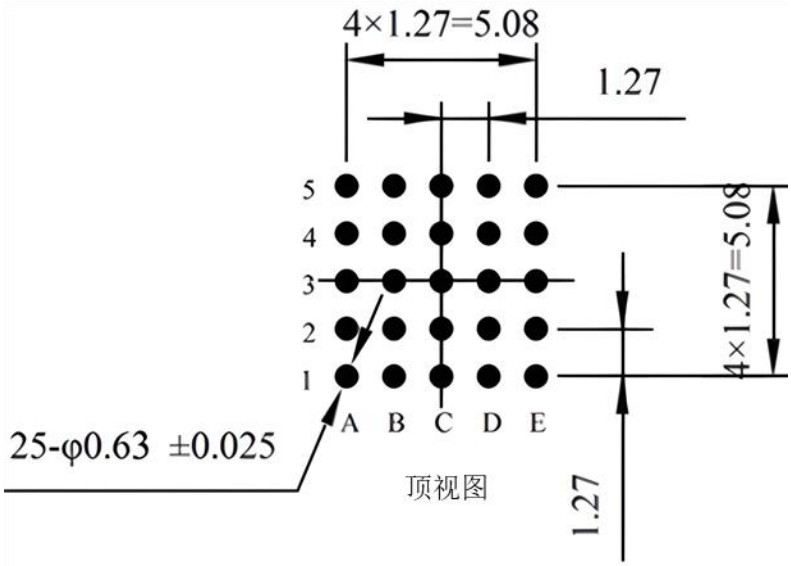


Figure 24 Recommended PCB pad size

Electro-Motive Explanation

Storage Requirements

General Requirements:Plastic-sealed packaged products (devices) must be stored in a clean, ventilated area free from corrosive gases, with temperature and relative humidity indicators. Plastic-sealed packaged products (devices) are shipped in anti-static sealed packaging. After opening, if assembly is not performed within 168 hours, they should be stored again in vacuum-sealed storage using anti-static bags.

Storage Conditions: Storag temperatur 10℃~25℃; relative humidity ≤ 70%RH. Effective storage period 18 months.

Recommended Soldering Process Conditions

① Product Pre-treatment

Before using the plastic-sealed module, it is recommended to bake at 125℃ for 48 hours, or refer to the requirements of IPC/JEDEC J-STD-033b "Operation, Packaging, Transportation and Use of Humidity Sensitive/Reflow Soldering Sensitive Surface Mount Devices" to ensure that the adsorbed moisture is completely removed. It is recommended to complete reflow soldering within 48 hours after baking.

② Soldering Solder Paste

For leaded soldering, Sn63Pb37 or Sn62Pb36Ag2 solder paste is recommended; for lead-free soldering, Sn96.5Ag3Cu0.5 solder paste is recommended. The solder paste should use grade 3 powder or above.

③ Soldering

The center of the module's solder pad should align with the printed solder paste, and the depth of the module's solder balls and pads pressed into the solder paste should be around 0.05mm.If the placement machine can adjust the pressure, it should ensure good contact between the solder pad and the solder paste without squeezing the solder paste out of the solder mask. Good contact with the solder paste can significantly reduce voids, and welding voids

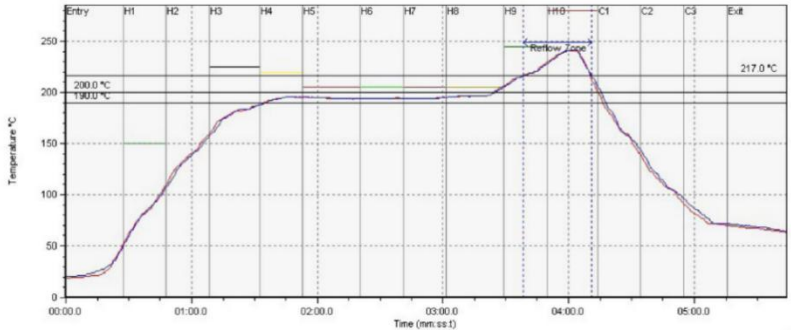
must not exceed 25%.

④ Recommended Soldering Curve

This product module can be compatible with both leaded soldering curves (as shown in Figure 16) and lead-free soldering curves (as shown in Figure 17). It is recommended to use a reflow soldering furnace with 9 or more temperature zones to achieve better uniformity of reflow temperature.

order number	project	condition	remarks
1	The slope of the rise in the maximum temperature of the preheating zone	≤3℃/s	-
2	Slope of maximum temperature decrease in preheating zone	≤4℃/s	-
3	Preheating zone time (130~160℃)	60s~120s	-
4	Maximum temperature in the reflux zone	210℃~230℃	-
5	Reflow zone time (≥183℃ time above Sn63Pb37)	30s~90s	-

Figure 25 Typical leaded reflow soldering curve and parameters



order number	project	condition	remarks
1	heating rate	< 3℃/s	-
2	Insulation zone	180℃~200℃	-
3	soaking time	60s~120s	-
4	Peak temperature	240℃~245℃	-
5	Liquefaction time (>217℃)	30s~90s	-
6	Rate of cooling	< 5℃/s	-

Figure 26 Typical leadless reflow soldering curve and parameters

Note 6: When using Denso, the above curve items can be optimized according to the actual layout of the device, but the peak temperature of the curve should not exceed 245° C. If the temperature of a thick or large metal device in the user's Denso needs to be higher than 245° C, the power module must be thermally shielded to ensure that the actual soldering temperature of the device is not higher than 245° C.

⑤ Cleaning

Clean with water-based cleaning agent, then dry. Cleaning process for welding, users can perform it according to actual conditions, but it is not recommended to use ultrasonic cleaning process.

⑥ Inspection

Inspect the appearance under a microscope to see if it meets the requirements.

⑦ X-ray Photography

Use X-RAY to detect the position of solder joints on the solder pads, check if the solder joint voids meet the requirements; whether there is a shor circuit situation. After inspecting 1-3 samples as the first batch, they can be subjected to batch reflow soldering.

Troubleshooting

If a suspected fault is found after the device is assembled, we recommend that you perform the following operations:

Open circuit: Check whether the solder joint has virtual soldering, less pin soldering, and cold sold ering.

Performance No Output: Check the output capacitance close to the module accessory.

Short Circuit: Use X-RAY to check for short circuits inside or outside the device.

Demolition process

Before removing the product module from the PCB, the PCB board needs to be baked at 125℃ for 48h to ensure that the modul is not affected.If it is not baked, there is a risk of delamination between the inside of the molded module and the bottom substrate, and in severe cases, the solder inside the module will melt and flow along the layered gap, causing the module to fail. It is recommended to use a BGA rework station to remove the module, not a hand-held heat gun (the temperature may exceed 245° C), and the product is only allowed to be reworked once

f) The relative humidity should be kept between 30%RH~70%RH as much as possible.

PRECAUTIONS

The device must be operated with anti-static measures. Anti-static gloves should be worn when taking the module to prevent the electrostatic impact of the human charge on the module and damage the module.

The following actions are recommended:

a) The device should be operated on an anti-static workbench or with finger covers;

b) Test equipment and appliances should be grounded;

c) Do not touch the device leads;

d) The device should be stored in a container made of anti-static material (e.g. anti-static box);

e) Avoid the use of plastic, rubber or silk fabrics that cause static electricity during production, testing, use and transfer;

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