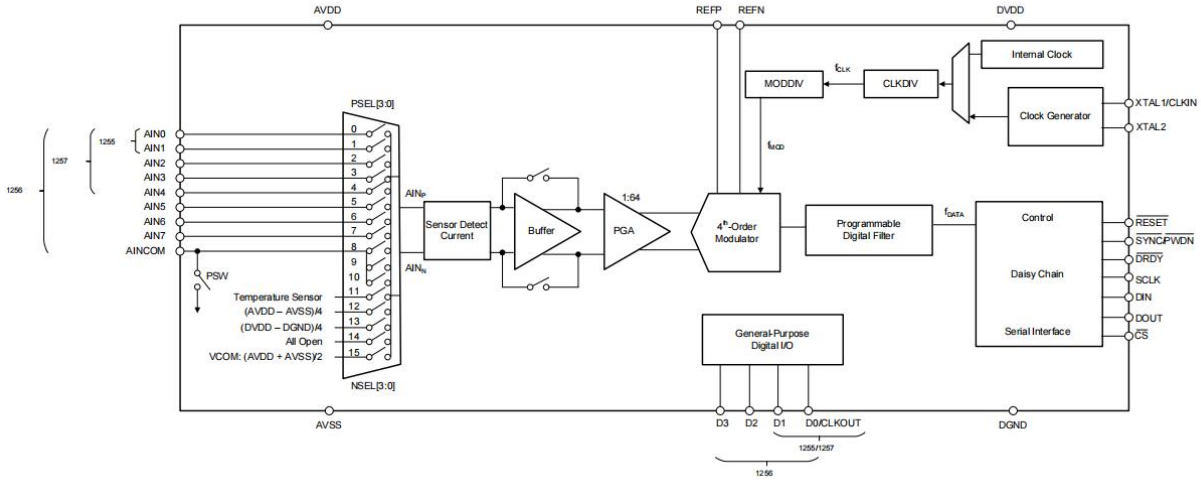
1. PRODUCT DESCRIPTION

The ADS1255-CN-M and ADS125-CN-M are extremely low-noise,60KSPS, 24-bit, delta-sigma (ΔΣ) analog-to-digital converters (ADCs) with an integrated multiplexer (mux), input buffer and programmable gain amplifier (PGA).

The input multiplexer can support four differential or eight single-ended input measurements. The sensor break detection circuit verifies the input connection continuity of the ADC. Selectable input buffers greatly increase the input impedance and in many cases eliminate the need for external buffers. Buffer input voltage ranges include AVSS. Low-noise PGAs offer gains from 1 to 64 to accommodate a variety of input signals. Programmable digital filters optimise ADC resolution (up to 23 bits without noise) and conversion rate (up to 60kSPS). Digital filters provide single-cycle stable conversion and suppress 50Hz and 60Hz interference signals.

The SPI-compatible serial interface requires only three wires to operate, simplifying connections to external controllers.The integrated calibration function supports self-calibration and systematic correction of offset and gain errors for all PGA gain settings.Four bidirectional digital I/O pins control external circuits.



2. FEATURES

- Up to 23 Bits Noise-Free Resolution
- Daisy Chain
- CRC/Lockout/Timeout Protection
- Clock/Reset/Register Map/Status Monitor
- Three Clocks (internal clock/XTAL/CLKIN) and Frequency Dividers
- Eight Analogue Inputs

  -Four differential or eight single-ended measurements
- Excellent DC performance

  - Offset Drift：84nV/°C (G = 1)

  - Gain Drift：1ppm/°C (G = 1)

- Nonlinear：1ppm (G = 1)

- Programmable Data Rate：2.5SPS to 60kSPS
- Single-cycle stable transitions(≤ 1000SPS)
- 50Hz and 60Hz Rejection
- High Impedance Input Buffer
- Differential Inpu PGA
- Integrated Sensor Breakage Detection
- Four General Purpose Inputs/Outputs
- Power Supply：

  -Analogue：

  -Single Channel: 4V to 5.5V

  -Dual Channel: ±2V to ±2.75V

  -Digital: 1.65V to 5.5V
- SPI™ Compatible Serial Interface

3. TYPICAL APPLICATIONS

- Scientific Instrumentation
- Test and Measurement

4. DEVICE INFORMATION

Table1 Device Information Sheet

Device	ADS1255-CN-M
Temperature Range	-55℃~125℃
Grade	Military
Package	SSOP-20
Dimensions(mm)	7.80x7.20

Device	ADS1256-CN-M
Temperature Range	-55℃~125℃
Grade	Military
Package	SSOP-28
Dimensions(mm)	10.20×7.80

5. PIN CONFIGURATION AND FUNCTION

ADS1255-CN-M/ADS1256-CN-M

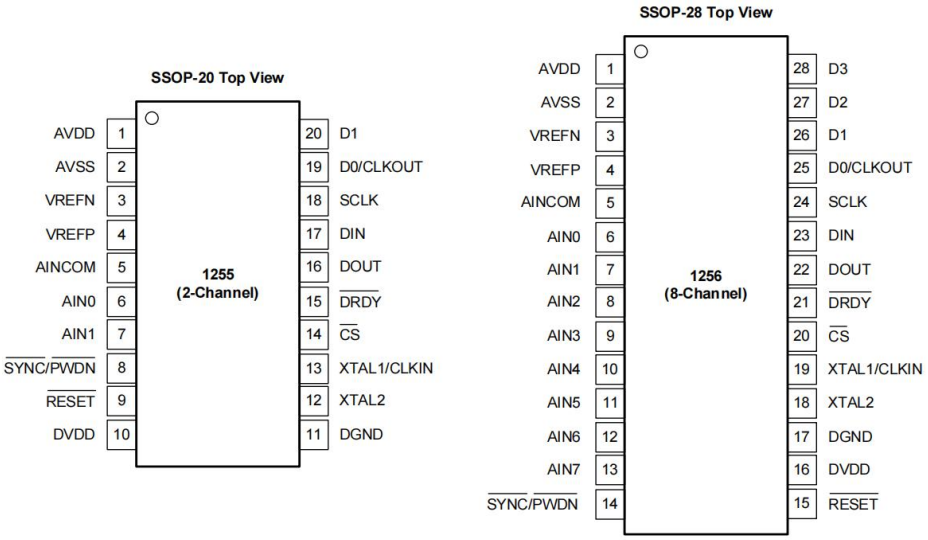


Figure 1 Pin Configuration (ADS1255-CN-M/ADS1256-CN-M)

Table 2 Pin Function (ADS1255-CN-M/ADS1256-CN-M)

Position		Name	Type	Description
ADS1255-CN-M	ADS1256-CN-M			
1	1	AVDD	Analog power supply	Positive analogue power supply
2	2	AVSS	Analog power supply	Negative analogue power supply
3	3	VREFN	Analog input	Negative reference input
4	4	VREFP	Analog input	Positive reference input
5	5	AINCOM	Analog input	Analog input common
6	6	AIN0	Analog input	Analog input 0
7	7	AIN1	Analog input	Analog input 1
-	8	AIN2	Analog input	Analog input 2
-	9	AIN3	Analog input	Analog input 3
-	10	AIN4	Analog input	Analog input 4
-	11	AIN5	Analog input	Analog input 5
-	12	AIN6	Analog input	Analog input 6
-	13	AIN7	Analog input	Analog input 7
8	14	$\overline{\text{SYNC}}$ / $\overline{\text{PWDN}}$	Digital input(1)(2)	Synchronization/power down input,active low
9	15	$\overline{\text{RESET}}$	Digital input(1)(2)	Reset input，active low
10	16	DVDD	Digital power supply	Digital power supply
11	17	DGND	Digital power supply	Digital ground
12	18	XTAL2	Digital(1)(2)	Crystal oscillator connection
13	19	XTAL1/CLKIN	Digital/Digital input	Crystal Oscillator Connection Circuit
14	20	$\overline{\text{CS}}$	Digital input(1)(2)	Chip select，active low
15	21	$\overline{\text{DRDY}}$	Digital output	Data ready output，active low
16	22	DOUT	Digital output	Serial data output
17	23	DIN	Digital input(1)(2)	Serial data input

18	24	SCLK	Digital input(1)(2)	Serial clock input
19	25	D0/CLKOUT	Digital IO(4)	Digital I/O 0 / clock outpu
20	26	D1	Digital IO(4)	Digital IO 1
-	27	D2	Digital IO(4)	Digital IO 2
-	28	D3	Digital IO(4)	Digital IO 3

(1) Schmitt-Trigger digital input.
(2) 5V tolerant digital input.
(3) Leave disconnected if external clock input is applied to XTAL1/CLKIN.
(4) Schmitt-Trigger digital input when the digital I/O is configured as an input.

6. SPECIFICATION

6.1 Absolute Maximum

Table 4 Absolute Maximum

Parameter	Description		Min	Max	Unit
Voltage	AVDD to AVSS		-0.3	6	V
	DVDD to DGND		-0.3	6	V
	AVSS to DGND		-2.8	0.3	V
	Analog input to AVSS		AVSS-0.3	AVDD+0.3	V
	Analog input	DIN,SCLK, $\overline{CS}$, $\overline{RESET}$, $\overline{SYNC}/\overline{PWDN}$, XTAL1/CLKIN to DGND	DGND-0.3	DGND+6.0	V
		D0/CLKOUT,D1,D2,D3	DGND-0.3	DVDD+0.3	V
Power Supply	Analog input	Discontinuous		100	mA
		Continuous	-10	10	mA
Tempera-ture	Operating temperature, T_A		-55	125	℃
	Junction temperature, T_J		-55	150	℃
	Storage temperature, T_{stg}		-65	150	℃
	Pin (Solder, 10 sec.)			300	℃

Note: Stresses in excess of the pressures listed in Table 4 may cause permanent damage to the device.These are absolute maximums only and do not imply that the device will operate properly under these or any other conditions than those described in Table 6.Prolonged exposure to absolute maximum rating conditions may affect device reliability.

6.2 ESD Rating

Table 5 ESD Rating

Parameter	Symbol	Description	Value	Unit
Electrostatic Discharges	$V_{(ESD)}$	Dummy(HBM), according to ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charge Device Model(CDM) , according to JEDEC specification JESD22-C101(2)	±1000	

Note1: JEDEC document JEP155 indicates that 500V HBMs are permitted to be safely manufactured using standard ESD controlled processes.
Note2: JEDEC document JEP157 indicates that 250V CDM allows for safe manufacturing using standard ESD controlled processes.

6.3 Recommended Working Conditions

Table 6 Recommended working conditions

PARAMETER	DESCRIPTION	SYMBOL	MIN	TYP	MAX	UNIT
Power Supply						
AVDD		V_{AVDD}		+2.5		V
AVSS		V_{AVSS}		-2.5		V
AVDD~AVSS			4		5.5	V
DVDD	DVDD GND	V_{DVDD}	1.65	1.8	5.5	V
Analog Input(1)						
Input Voltage		$V_{(AINX)}$	AVSS		AVDD	V
Digital Input						
Digital Input Voltage	DIN,SCLK, $\overline{CS}$, $\overline{RESET}$, $\overline{SYNC}$ / $\overline{PWDN}$,XTAL1/CLKIN to DGND	V_{DIG}	DGND		5.5	V
	D0/CLKOUT,D1,D2,D3		DGND		DVDD	V
Temperature Range						
Operating Temperature		T_A	-55		125	℃

6.4 Thermal Information

Table 7 Thermal Information

PARAMETER	SYMBOL	SSOP-20	QFN-20	SSOP-28	UNIT
Thermal resistance of junction to air	$T_{\theta JA}$	66.4	35.1	56.8	℃/W
Thermal resistance of junction to PCB surface	$R_{\theta JB}$	40.2	13.3	32.9	℃/W
Characteristic parameters knotted to the top of the package	ψ_{JT}	1.9	0.3	2.6	℃/W
Characteristic parameters of the junction to the surface of the PCB	ψ_{JB}	38.0	13.3	31.2	℃/W
Thermal resistance of the junction to the chip package surface	$R_{\theta JC(top)}$	25.8	15.0	24.4	℃/W
Thermal resistance of the junction to the bottom of the chip package	$R_{\theta JC(bot)}$	—	—	—	℃/W

6.5 Electrical Characteristics

Table 8 lists the ADS1255/1256-CN-M $T_{A=}$ −55°C to 125°C, AVDD = 5V, DVDD = 1.8V, f_{CLK}=7.68MHz (crystal oscillator), CLKOUT off, PGA = 1, buffer on and V_{REF}= 2.5V, unless otherwise noted.

Table 8 Electrical Characteristics

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
Analog Input					
Full-scale input voltage （AIN_P– AIN_N）			±2V_{REF}/ PGA		V
Absolute input voltage (AIN0-7, AINCOM to AVSS)	Buffer off	AVSS – 0.1		AVDD + 0.1	V
	Buffer on	AVSS		AVDD – 2.0	V
Programmable gain amplifier		1		64	
Differential input impedance	Buffer off, PGA = 1, 2, 4, 8, 16		80 / PGA		kΩ
	Buffer off, PGA = 32, 64		3.7		kΩ
	Buffer on, f_{DATA} ≤ 50Hz(1)		80		MΩ
Sensor detect current sources	SDCS[1:0] = 01		0.5		μA
	SDCS[1:0] = 10		2		μA
	SDCS[1:0] = 11		10		μA

System Performance					
Resolution		24			Bit
No missing codes	All data rates and PGA settings	24			Bit
Data rate(f_{DATA})	f_{CLK} = 7.68MHz	2.5		60,000	SPS
Integral nonlinearity	Differential input, PGA = 1		3	9	ppm
	Differential input, PGA = 64		3		ppm
Offset error	After calibration		On the level of the noise		
Offset drift	PGA = 1		±80		nV/°C
	PGA = 64		±170		nV/°C
Gain error	After calibration, PGA = 1, Buffer on		±0.003		%
	After calibration, PGA = 64, Buffer on		±0.07		%
Gain drift	PGA = 1		±0.9		ppm/°C
	PGA = 64		±0.4		ppm/°C
Common-mode rejection	f_{CM} = 60Hz, f_{DATA} = 30kSPS	100	113		dB
	DC, f_{DATA}= 30kSPS	127	138		dB
Normal-mode rejection	External clock, ODR= 10SPS, 50Hz ± 1Hz and 60Hz ± 1Hz	104	123		dB
THD	f_{DATA} = 30kSPS, input = −0.5dbFSR, 10Hz		106		dB
Power Supply Rejection Ratio					
AVDD power-supply rejection	±5% Δ in AVDD	92	97		dB
DVDD power-supply rejection	±10% Δ in DVDD	100	106		dB
Voltage Reference Inputs					
Reference input voltage(V_{REF})	V_{REF}≤ VREFP – VREFN	0.5	2.5	2.6	V
Negative reference input (VREFN)	Buffer off	AVSS − 0.1		VREFP − 0.5	V
	Buffer on	AVSS		VREFP − 0.5	V
Positive reference input (VREFP)	Buffer off	VREFN + 0.5		AVDD + 0.1	V
	Buffer on	VREFN + 0.5		AVDD − 2.0	V
Voltage reference impedance	f_{CLK}= 7.68MHz		1		MΩ
Digital Input/Output					
V_{IH}	DIN, SCLK, XTAL1/CLKIN, $\overline{SYNC}$/ $\overline{PWDN}$,$\overline{CS}$,$\overline{RESET}$	0.7 DVDD		5.25	V
	D0/CLKOUT, D1, D2, D3	0.7 DVDD		DVDD	V

V_{IL}		DGND		0.3 DVDD	V
V_{OH}	I_{OH}= 5mA	0.7 DVDD			V
V_{OL}	I_{OL}= 5mA			0.3 DVDD	V
Input hysteresis			0.5		V
Input leakage	0 < $V_{DIGITAL\ INPUT}$ < DVDD			±10	µA
Master clock rate	External crystal between XTAL1 and XTAL2	1	7.68	10	MHz
	Internal oscillator		7.68		MHz
	Frequency variation at room temperature			±1	%
	Frequency variation within voltage and temperature range			±6	%
	Duty cycle	40	50	60	%
	External oscillator driving CLKIN	0.1	7.68	10	MHz
Power-Supply					
AVDD		4		5.5	V
DVDD		1.65		5.5	V
AVDD current	Power-down mode			5	µA
	Standby mode		3		µA
	Normal mode, PGA = 1, Buffer off		6	8	mA
	Normal mode, PGA = 64, Buffer off		14	18	mA
	Normal mode, PGA = 1, Buffer on		11	14	mA
	Normal mode, PGA = 64, Buffer on		27	35	mA
DVDD current	Power-down mode			3	µA
	Standby mode, CLKOUT off, DVDD = 3.3V		105		µA
	Normal mode, CLKOUT off, DVDD = 3.3V		2	3	mA
Power dissipation	Normal mode, PGA = 1, Buffer off, DVDD = 3.3V		34	46	mW
	Standby mode, DVDD = 3.3V		0.4		mW
Temperature Sensor					
Sensor voltage	T_A= 25°C		136.8		mV
Temperature coefficient			378		V/°C

Temperature Range					
Specified		−55		125	°C
Operating		−55		125	°C
Storage		−60		150	°C

(1) See text for more information on input impedance.
(2) SPS = samples per second.
(3) FSR = full-scale range = $4V_{REF}$/PGA.
(4) f_{CM} is the frequency of the common-mode input signal.
(5) Placing a notch of the digital filter at 60Hz (setting f_{DATA} = 60SPS, 30SPS, 15SPS, 10SPS, 5SPS, or 2.5SPS) will further improve the common-mode rejection of this frequency.
(6) The reference input range with Buffer on is restricted only if self-calibration or gain self-calibration is to be used. If using system calibration or writing calibration values directly to the registers, the entire Buffer off range can be used.

6.6 Serial Interface Timing

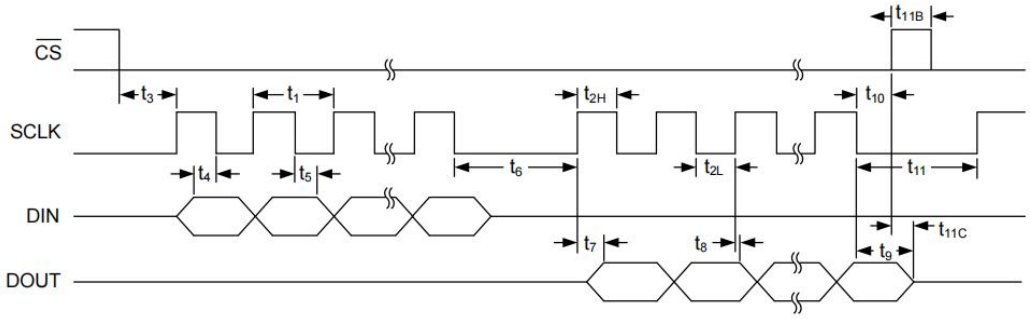


Figure 3 Serial Interface Timing

Table 9 Serial Interface Timing Characteristics

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT
SCLK period	t_1		3			t_{CLK}
					10	t_{DATA}
SCLK pulse width: high	t_{2H}		200			ns
					9	t_{DATA}
SCLK pulse width: low	t_{2L}		200			ns
$\overline{CS}$ low to first SCLK: setup time(3)	t_3		0			ns
Valid DIN to SCLK falling edge: setup time	t_4		50			ns
Valid DIN to SCLK falling edge: hold time	t_5		50			ns
Delay from last SCLK edge for DIN to first SCLK rising edge for DOUT: RDATA, RDATAC,RREG Commands	t_6		4			t_{CLK}
SCLK rising edge to valid new DOUT: propagation delay(4)	t_7				50	ns
SCLK rising edge to DOUT invalid: hold time	t_8		0			ns
Last SCLK falling edge to DOUT high impedance(5)	t_9		6		10	t_{CLK}
$\overline{CS}$ low after final SCLK falling edge	t_{10}		8			t_{CLK}
Final SCLK falling edge of command to first SCLK,rising edge of next command. RREG，4WREG，RDATA	t_{11}		4			t_{CLK}
Final SCLK falling edge of command to first SCLK,rising edge of next command. RDATAC，$\overline{SYNC}$						t_{CLK}

Final SCLK falling edge of command to first SCLK,rising edge of next command. RDATAC，$\overline{\text{RESET}}$，STANDBY, SELFOCAL,SYSOCAL, SELFGCAL, SYSGCAL, SELFCAL		Wait for $\overline{\text{DRDY}}$ to go low

Note 1: t_{CLK} = master clock period = $1/f_{CLK}$.

Note 2: t_{DATA} = output data period = $1/f_{DATA}$.

Note 3: $\overline{\text{CS}}$ can be tied low.

Note 4: DOUT load = 20pF || 100kΩ to DGND

Note 5: When $\overline{\text{CS}}$ is high level,DOUT immediately becomes high impedance.

6.7 SCLK Reset Timing

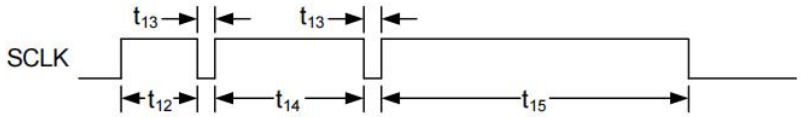


Figure 4 SCLK Reset Timing

Table 10 SCLK Reset Timing Characteristics

PARAMETER	SYMBOL	MIN	MAX	UNIT
SCLK reset pattern, first high pulse	t_{12}	300	500	t_{CLK}
SCLK reset pattern, low pulse	t_{13}	6		t_{CLK}
SCLK reset pattern, second high pulse	t_{14}	550	750	t_{CLK}
SCLK reset pattern, third high pulse	t_{15}	1050	1250	t_{CLK}

Note: t_{CLK} = master clock period = $1/f_{CLK}$.

6.8 $\overline{\text{RESET}}$, $\overline{\text{SYNC}}/\overline{\text{PWDN}}$ Timing

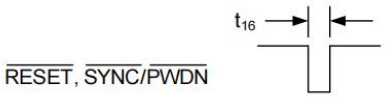


Figure 5 $\overline{\text{RESET}}$, $\overline{\text{SYNC}}/\overline{\text{PWDN}}$ Timing

Table 11 $\overline{\text{RESET}}$, $\overline{\text{SYNC}}/\overline{\text{PWDN}}$ Timing Characteristics

PARAMETER	SYMBOL	MIN	MAX	UNIT
$\overline{\text{RESET}}$, $\overline{\text{SYNC}}/\overline{\text{PWDN}}$, pulse width	t_{16}	2		t_{CLK}

Note: t_{CLK} = master clock period = $1/f_{CLK}$.

6.9 $\overline{\text{DRDY}}$ Update Timing

Figure 6 $\overline{\text{DRDY}}$ Update Timing

Table 12 $\overline{DRDY}$ Update Timing Characteristics

PARAMETER	SYMBOL	MIN	MAX	UNIT
Conversion data invalid while being updated (DRDY shown with no data retrieval)	t_{17}	16		t_{CLK}

Note: t_{CLK} = master clock period = $1/f_{CLK}$.

7. TYPICAL CHARACTERISTICS

T_A = 25°C, AVDD = 5V, DVDD = 1.8V, f_{CLK} = 7.68MHz, PGA = 1, and V_{REF} = 2.5V, unless otherwise noted.

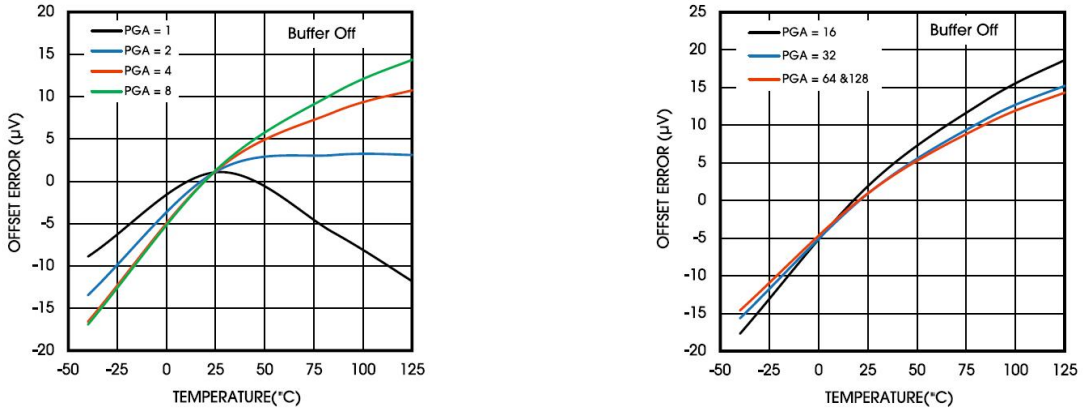


Figure 7 Offset Error vs. Temperature

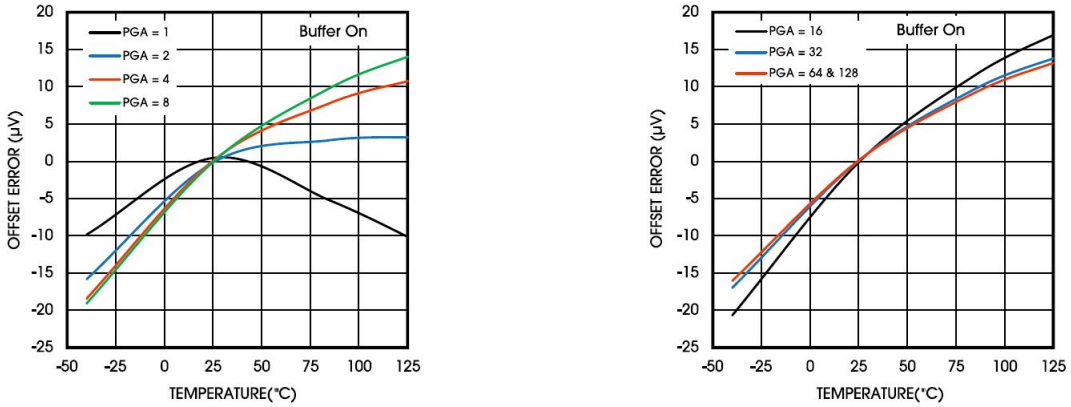


Figure 8 Offset Error vs. Temperature

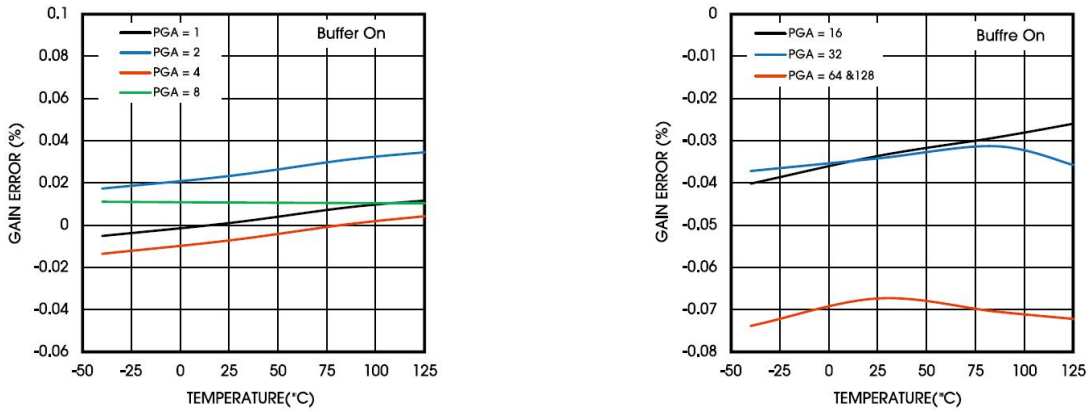


Figure 9 Gain Error vs. Temperature

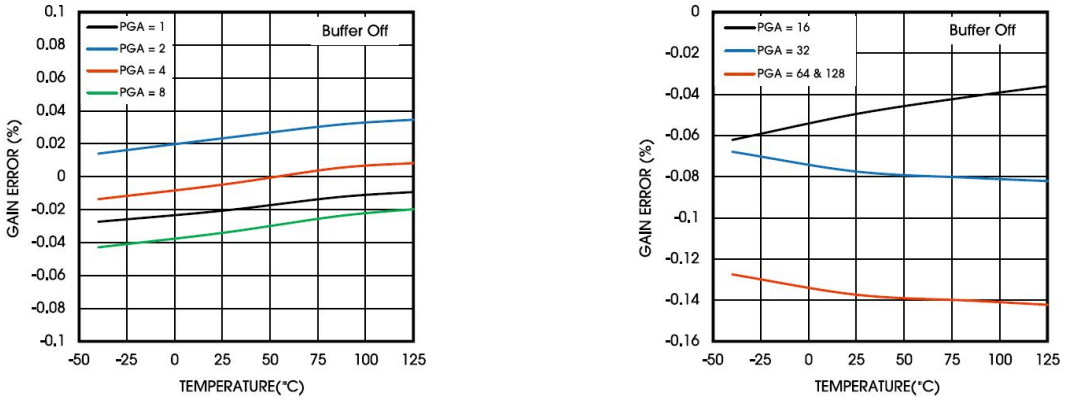


Figure 10 Gain Error vs. Temperature

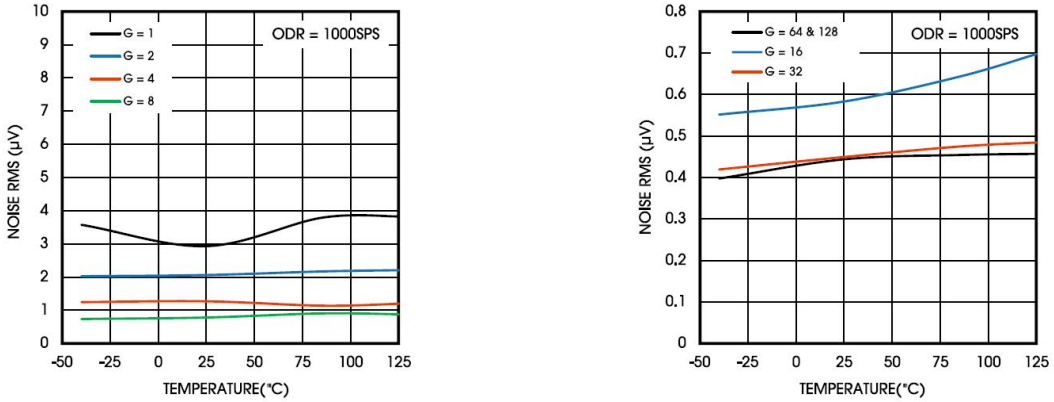
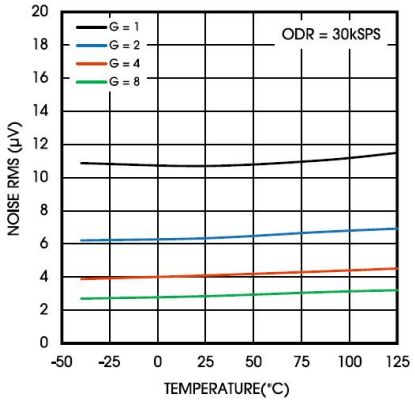


Figure 11 Noise RMS vs. Temperature



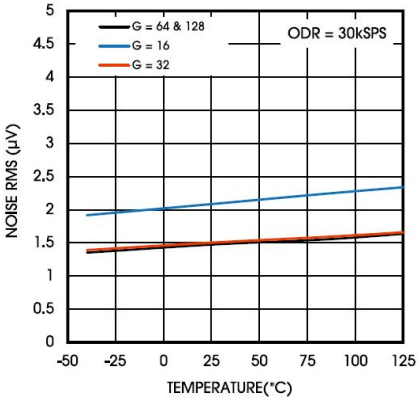


Figure 12 Noise RMS vs. Temperature

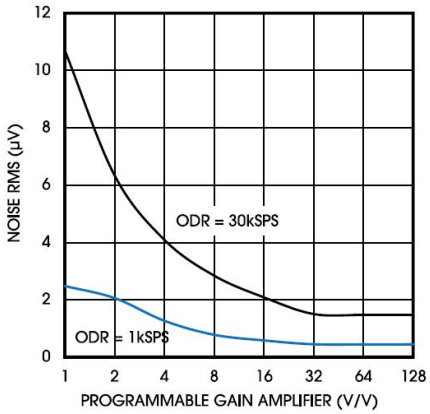


Figure 13 Noise RMS vs. PGA

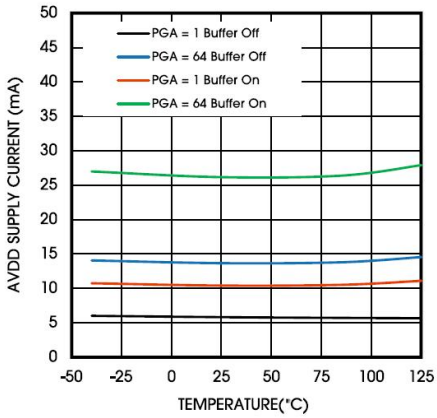


Figure 14 Supply Current vs. Temperature

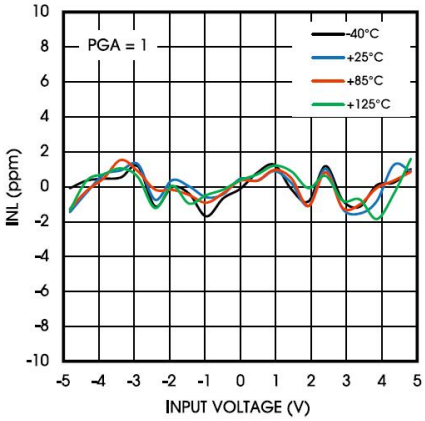


Figure 15 Integral nonlinearity vs. inputs

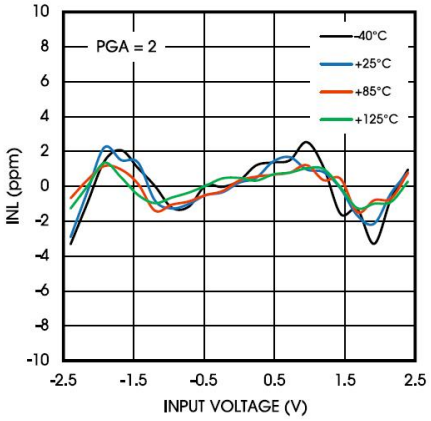


Figure 16 Integral nonlinearity vs. inputs

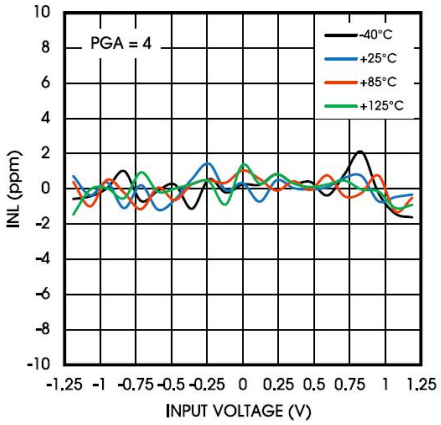


Figure 17 Integral nonlinearity vs. inputs

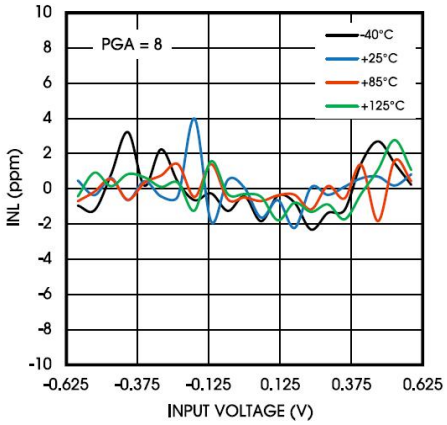


Figure 18 Integral nonlinearity vs. inputs

8. PARAMETER MEASUREMENT INFORMATION

8.1 Noise Performance

The ADS1255/1256-CN-M offer outstanding noise performance thatcan be optimized by adjusting the data rate or PGAsetting.As the averaging is increased by reducing the data rate,the noise drops correspondingly. The PGA reduces the input-referred noise when measuring lower level signals.Table 13 through Table 19 summarizethe typical noise performance with the inputs shorted externally. In all four tables, the following conditions apply: T_A= 25°C, AVDD = 5V, DVDD =1.8V, V_{REF}=2.5V, and f_{CLKIN} = 7.68MHz. Table 13 and Table 17 show the root mean square(RMS) values of the input reference noise. Table 15 and Table 19 show the effectivenumber of bits of resolution (ENOB), using the noise data from Table 13 and Table 17. ENOB is defined as:

$$ENOB = \frac{\ln（FSR/RMS\ Noise）}{\ln（2）} \qquad （1）$$

• where FSR is the full-scale range.: $FSR = 4 \times V_{REF} / Gain$.

Table 15 and Table 19 shows the noise-free bits of resolution. It is calculated with the same formula as ENOB except the peak-to-peak noise value isused instead of rms noise.

Table 13 Input Referred Noise With Buffer On (μV_{RMS})

Data Rate (SPS)	PGA Gain						
	1	2	4	8	16	32	64
2.5	0.232	0.069	0.089	0.051	0.040	0.028	0.028
5	0.212	0.138	0.089	0.079	0.052	0.044	0.038
10	0.316	0.177	0.124	0.084	0.072	0.053	0.056
15	0.350	0.215	0.145	0.103	0.081	0.068	0.071
25	0.464	0.276	0.183	0.128	0.110	0.096	0.087
30	0.438	0.285	0.189	0.152	0.114	0.092	0.095
50	0.570	0.379	0.263	0.198	0.150	0.123	0.119
60	0.660	0.398	0.271	0.192	0.152	0.114	0.117
100	0.820	0.539	0.356	0.254	0.192	0.147	0.149
500	1.757	1.111	0.775	0.580	0.449	0.352	0.344
1000	2.932	1.906	1.197	0.851	0.598	0.448	0.438
2000	3.558	2.218	1.509	1.095	0.812	0.585	0.587

3750	5.073	3.124	2.104	1.506	1.124	0.815	0.805
7500	7.090	4.414	3.012	2.185	1.606	1.156	1.150
15,000	9.957	5.953	3.959	2.821	2.071	1.493	1.471
30,000	10.848	6.323	4.103	2.870	2.098	1.494	1.490
60,000							

Table 14 Input Referred Noise With Buffer On (μV_{PP})

Data Rate (SPS)	PGA Gain						
	1	2	4	8	16	32	64
2.5	0.789	0.395	0.296	0.197	0.148	0.117	0.105
5	0.789	0.493	0.296	0.271	0.234	0.197	0.182
10	1.579	0.789	0.592	0.419	0.358	0.240	0.250
15	1.381	0.888	0.839	0.469	0.481	0.333	0.353
25	1.973	1.381	0.987	0.765	0.592	0.425	0.436
30	2.368	1.381	0.987	0.715	0.580	0.512	0.541
50	2.762	1.973	1.431	1.036	0.777	0.691	0.668
60	3.946	2.072	1.529	1.159	0.814	0.641	0.600
100	4.538	3.256	2.170	1.579	1.295	0.987	0.996
500	13.417	7.991	6.117	3.823	3.305	2.534	2.387
1000	63.536	33.642	7.498	10.778	8.620	3.231	3.482
2000	26.638	16.279	10.704	7.991	5.697	4.033	4.342
3750	37.095	23.678	15.095	11.099	8.928	6.037	5.740
7500	54.656	32.952	22.642	16.130	11.580	9.009	8.674
15,000	78.137	47.849	31.077	22.691	15.945	11.697	11.693
30,000	84.451	50.710	34.086	23.678	18.042	12.758	11.492
60,000							

Table 15 Effective Number of Bits (ENOB, rms) With Buffer On

Data Rate (SPS)	PGA Gain						
	1	2	4	8	16	32	64
2.5	25.4	26.1	24.7	24.6	23.9	23.4	22.4
5	25.5	25.1	24.7	23.9	23.5	22.8	22.0
10	24.9	24.8	24.3	23.8	23.0	22.5	21.4
15	24.8	24.5	24.0	23.5	22.9	22.1	21.1
25	24.4	24.1	23.7	23.2	22.4	21.6	20.8
30	24.4	24.1	23.7	23.0	22.4	21.7	20.7
50	24.1	23.7	23.2	22.6	22.0	21.3	20.3
60	23.9	23.6	23.1	22.6	22.0	21.4	20.3
100	23.5	23.1	22.7	22.2	21.6	21.0	20.0
500	22.4	22.1	21.6	21.0	20.4	19.8	18.8
1000	21.7	21.3	21.0	20.5	20.0	19.4	18.4
2000	21.4	21.1	20.7	20.1	19.6	19.0	18.0
3750	20.9	20.6	20.2	19.7	19.1	18.5	17.6
7500	20.4	20.1	19.7	19.1	18.6	18.0	17.1
15,000	19.9	19.7	19.3	18.8	18.2	17.7	16.7

30,000	19.8	19.6	19.2	18.7	18.2	17.7	16.7
60,000	19.5	19.3	19.1	18.7	18.2	18.1	17.1

Table 16 Noise-Free Resolution (Bits) With Buffer On

Data Rate (SPS)	PGA Gain						
	1	2	4	8	16	32	64
2.5	25.4	25.6	24.8	25.1	24.6	23.9	23.1
5	25.4	25.0	24.9	24.7	24.2	23.4	22.5
10	25.3	24.9	24.5	24.3	23.6	23.0	22.0
15	24.7	24.6	24.2	24.0	23.4	23.0	21.8
25	24.5	24.2	24.0	23.6	23.1	22.3	21.3
30	24.4	24.2	23.8	23.5	22.9	22.3	21.3
50	24.1	23.8	23.5	23.1	22.5	21.9	20.9
60	24.0	23.8	23.4	23.0	22.5	21.9	20.9
100	23.6	23.4	23.0	22.6	22.1	21.5	20.5
500	22.5	22.3	21.9	21.5	20.9	20.3	19.3
1000	21.7	21.8	21.4	21.0	20.5	20.0	19.0
2000	21.5	21.2	20.9	20.5	20.0	19.5	18.5
3750	21.0	20.8	20.5	20.0	19.6	19.0	18.1
7500	20.5	20.2	19.9	19.5	19.0	18.5	17.6
15,000	20.0	19.8	19.5	19.1	18.7	18.2	17.2
30,000	19.9	19.7	19.5	19.1	18.6	18.2	17.2
60,000	19.5	19.4	19.2	19.0	18.6	18.1	17.2

Table 17 Input Referred Noise With Buffer Off (μV_{RMS})

Data Rate (SPS)	PGA Gain						
	1	2	4	8	16	32	64
2.5	0.219	0.097	0.088	0.035	0.025	0.020	0.017
5	0.221	0.150	0.080	0.047	0.033	0.028	0.026
10	0.242	0.156	0.102	0.061	0.049	0.036	0.038
15	0.365	0.194	0.126	0.075	0.055	0.038	0.043
25	0.421	0.255	0.152	0.099	0.069	0.060	0.059
30	0.451	0.266	0.172	0.108	0.079	0.062	0.062
50	0.548	0.347	0.213	0.144	0.105	0.082	0.080
60	0.587	0.337	0.223	0.149	0.107	0.082	0.078
100	0.774	0.444	0.293	0.195	0.136	0.105	0.106
500	1.650	1.002	0.640	0.427	0.310	0.241	0.236
1000	2.897	1.404	0.893	0.607	0.422	0.308	0.302
2000	3.437	2.045	1.286	0.844	0.585	0.419	0.411
3750	4.861	2.831	1.742	1.161	0.808	0.578	0.566
7500	6.869	4.048	2.516	1.662	1.163	0.825	0.812
15,000	9.580	5.504	3.326	2.178	1.518	1.058	1.042
30,000	10.551	5.888	3.471	2.232	1.526	1.070	1.041
60,000							

Table 18 Input Referred Noise With Buffer Off (μV_{PP})

Data Rate (SPS)	PGA Gain						
	1	2	4	8	16	32	64
2.5	0.592	0.395	0.247	0.123	0.111	0.074	0.080
5	0.987	0.296	0.296	0.148	0.173	0.142	0.114
10	1.184	0.789	0.493	0.321	0.271	0.191	0.170
15	1.579	0.888	0.543	0.395	0.284	0.228	0.232
25	2.170	1.184	0.839	0.493	0.407	0.345	0.306
30	2.368	1.480	0.740	0.592	0.395	0.339	0.328
50	2.960	1.874	1.233	0.765	0.654	0.444	0.461
60	3.354	2.072	1.233	0.863	0.592	0.444	0.470
100	4.538	2.762	1.727	1.184	0.839	0.672	0.637
500	12.431	6.709	4.538	3.157	2.183	1.739	1.583
1000	17.561	10.754	18.005	4.292	3.182	3.607	2.205
2000	24.270	14.700	9.027	6.265	4.020	3.052	3.077
3750	38.082	20.126	12.825	9.126	5.956	4.193	4.082
7500	53.275	31.274	20.422	12.973	8.669	6.462	6.782
15,000	73.204	42.719	25.059	16.500	11.358	8.164	7.824
30,000	87.214	49.132	29.104	17.265	12.344	8.620	8.606
60,000							

Table 19 Effective Number of Bits (ENOB, rms) With Buffer Off

Data Rate (SPS)	PGA Gain						
	1	2	4	8	16	32	64
2.5	23.6	23.6	23.0	22.6	22.0	21.3	20.5
5	23.6	23.3	23.0	22.1	21.3	20.6	19.7
10	22.6	22.6	22.0	21.5	20.7	20.3	19.3
15	22.8	22.4	21.5	21.3	20.3	19.8	18.8
25	22.3	21.8	21.3	20.6	20.0	19.5	18.5
30	22.0	21.8	21.3	20.7	20.0	19.2	18.1
50	21.8	21.3	20.7	20.2	19.6	18.8	17.8
60	21.3	21.2	20.6	20.0	19.6	18.9	18.0
100	21.1	20.6	20.1	19.6	18.9	18.3	17.3
500	19.5	19.3	18.6	18.3	17.5	16.9	16.0
1000	17.3	17.2	18.3	16.8	16.1	16.6	15.5
2000	18.5	18.2	17.8	17.3	16.7	16.2	15.1
3750	18.0	17.7	17.3	16.8	16.1	15.7	14.7
7500	17.5	17.2	16.8	16.2	15.7	15.1	14.1
15,000	17.0	16.7	16.3	15.7	15.3	14.7	13.7
30,000	16.9	16.6	16.2	15.7	15.1	14.6	13.7
60,000	16.5	16.3	16.0	15.7	15.1	15.0	14.0

Table 20 Noise-Free Resolution (Bits) With Buffer Off

Data Rate (SPS)	PGA Gain						
	1	2	4	8	16	32	64
2.5	24.0	23.6	23.3	23.3	22.4	22.0	20.9
5	23.3	24.0	23.0	23.0	21.8	21.1	20.4
10	23.0	22.6	22.3	21.9	21.1	20.6	19.8
15	22.6	22.4	22.1	21.6	21.1	20.4	19.4
25	22.1	22.0	21.5	21.3	20.6	19.8	19.0
30	22.0	21.7	21.7	21.0	20.6	19.8	18.9
50	21.7	21.3	21.0	20.6	19.9	19.4	18.4
60	21.5	21.2	21.0	20.5	20.0	19.4	18.3
100	21.1	20.8	20.5	20.0	19.5	18.8	17.9
500	19.6	19.5	19.1	18.6	18.1	17.5	16.6
1000	19.1	18.8	17.1	18.2	17.6	16.4	16.1
2000	18.7	18.4	18.1	17.6	17.2	16.6	15.6
3750	18.0	17.9	17.6	17.1	16.7	16.2	15.2
7500	17.5	17.3	16.9	16.6	16.1	15.6	14.5
15,000	17.1	16.8	16.6	16.2	15.7	15.2	14.3
30,000	16.8	16.6	16.4	16.1	15.6	15.1	14.1
60,000	16.4	16.4	16.3	16.0	15.6	15.1	14.2

9. OVERVIEW

9.1 Overview

The ADS1255-CN-M and ADS1256-CN-M are very low-noise A/D converters. The ADS1255-CN-M supports one differential or two single-ended inputs and has two general-purpose digital I/Os. The ADS1256-CN-M supports four differential or eight single-ended inputs and has four general-purpose digital I/Os. Otherwise, the two units are identical and are referred to together in this data sheet as the ADS1255/1256-CN-M. Figure 5 shows a block diagram of the ADS1256-CN-M. The input multiplexer selects which input pins are connected to the A/D converter. Selectable current sources within the input multiplexer can check for open or short-circuit conditions on the external sensor. A selectable onboard input buffer greatly reduces the input circuitry loading by providing up to 80MΩ of impedance. A low-noise PGA provides a gain of 1, 2, 4, 8, 16, 32, or 64. The ADS1255/1256-CN-M converter is comprised of a 4th-order, delta-sigma modulator followed by a programmable digital filter. The modulator measures the amplified differential input signal, V_{IN} = (AIN_P – AIN_N), against the differential reference, V_{REF} = (VREFP – VREFN). The differential reference is scaled internally by a factor of two so that the full-scale input range is ±2V_{REF} (for PGA = 1).

The digital filter receives the modulator signal and provides a low-noise digital output. The data rate of the filter is programmable from 2.5SPS to 30kSPS and allows tradeoffs between resolution and speed.

Communication is done over an SPI-compatible serial interface with a set of simple commands providing control of the ADS1255/1256-CN-M. Onboard registers store the various settings for the input multiplexer, sensor detect current sources, input buffer enable, PGA setting, data rate, etc. Either an external crystal or clock oscillator can be used to provide the clock source. General-purpose digital I/Os provide static read/write control of up to four pins. One of the pins can also be used to supply a programmable clock output.

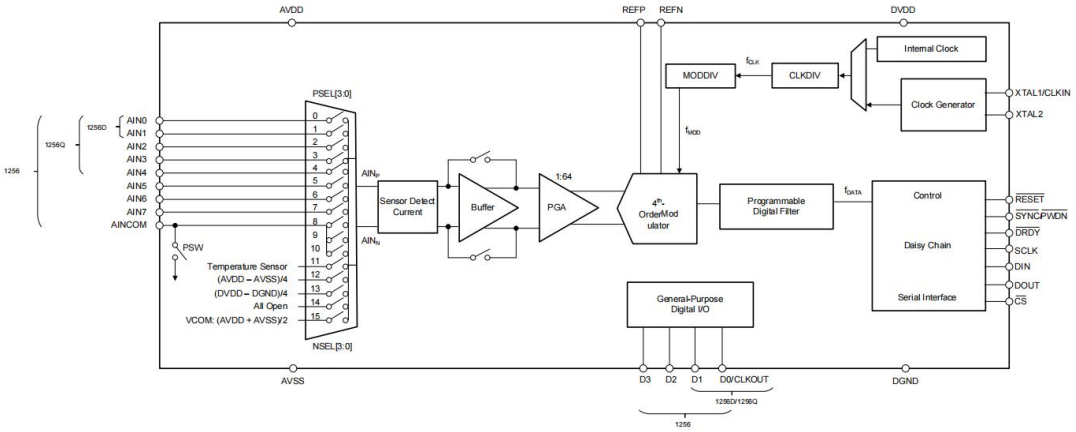


Figure 19 Block Diagram

9.1.1 Input Multiplexer

Figure 20 shows a simplified diagram of the input multiplexer. This flexible block allows any analog input pin to be connected to either of the converter differential inputs. That is, any pin can be selected as the positive input (AIN_P); likewise, any pin can be selected as the negative input (AIN_N). The pin selection is controlled by the multiplexer register.

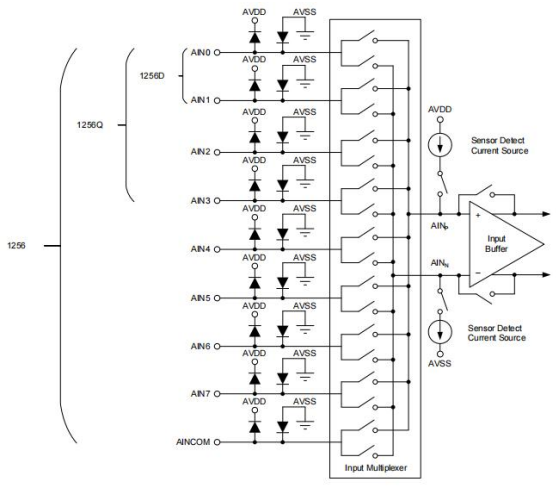
The ADS1256-CN-M offers nine analog inputs, which can be configured as four independent differential inputs , eight single-ended inputs, or a combination of differential and single-ended inputs.The ADS1255-CN-M offers three analog inputs, which can be configured as one differential input or two single-ended inputs. When using the ADS1255-CN-M and programming the input, make sure to select only the available inputs when programming the input multiplexer register.

In general, there are no restrictions on input pin selection.However, for optimum analog performance, the following recommendations are made:

1. For differential measurements use AIN0 through AIN7, preferably adjacent inputs. For example, use AIN0 and AIN1. Do not use AINCOM.
2. For single-ended measurements use AINCOM as common input and AIN0 through AIN7 as single-ended inputs.
3. Leave any unused analog inputs floating. This minimizes the input leakage current.

ESD diodes protect the analog inputs. To keep these diodes from turning on, make sure the voltages on the input pins do not go below AVSS by more than 100mV,and likewise do not exceed AVDD by more than 100mV:−100mV < (AIN0 − 7 and AINCOM) < AVDD + 100mV.

When using ADS1255/1256-CN-M for single-ended measurements,it is important to note that common input AIN COM does not need to be tied to ground. For example, AINCOM can be tied to a midpoint reference such as +2. 5V or even AVDD.



9.1.2 Temperature Sensor

The ADC has an internal temperature sensor. The temperature sensor consists of two internal diodes, one of which has a current density 80 times that of the other. The difference in diode current density produces a differential output voltage proportional to the absolute temperature. The temperature sensor readings are converted by the ADC. See Table 39 for information on register settings to select the temperature sensor to be used for the measurement. Equation 2 shows how the temperature sensor reading is converted to degrees Celsius (˚C):

$$\text{Temperature (°C)} = [(\text{Temperature Reading } (\mu V) - 116{,}926) / 378\mu V/°C] + 25°C \qquad (2)$$

The temperature sensor was measured with the PGA on, G = 1, burn-in current source disabled and AC excitation mode disabled. The internal temperature closely tracks the PCB temperature due to the low package-to-PCB thermal resistance. Note that device self-heating increases the internal temperature relative to the surrounding PCB. Also note that the input buffer should be turned on (BUFEN=1) so that the measured temperature data conforms to Equation 2.

9.1.3 Power Readback

The supply voltage is read through the appropriate input multiplexer selection. The supply voltage is divided to reduce the voltage level to within the ADC input range. The analogue and digital power supply readback levels are scaled by Equations 3 and 4, respectively:

$$\text{Analog supply (V)} = (AVDD - AVSS) / 4 \qquad (3)$$

$$\text{Digital supply (V)} = DVDD / 4 \qquad (4)$$

Perform the measurement with PGA enabled, G = 1, and burn-in current source disabled. See Table 39 for the register settings used to measure the supply voltage.

9.1.4 Open input

This configuration turns on all inputs. Use this configuration to test the functionality of the transducer burn-in current source and the PGA output monitor. When the inputs are turned on, the current source drives the PGA inputs to full scale, causing the PGA monitor to alarm and clipping the conversion data. See Table 39 for register settings to turn on all inputs.

9.1.5 Internal VCOM Connections

For this multiplexer configuration, all inputs are turned on and the PGA inputs are connected to the defined internal VCOM voltage: (AVDD + AVSS)/2. Use this mode to measure ADC noise performance and out-of-regulation voltages, or to calibrate the inputs with short-circuit offsets. See Table 39 for register settings for the internal VCOM connection.

Figure 15 shows a simplified diagram of the AD1255/1256-CN-M input structure, where the external sensor is modelled as a resistance between the two input pins R_{SENS}.When SDCS are enabled, they source I_{SDC} to the input pin connected to AIN_P and absorb I_{SDC} from the input pin connected to AIN_N.Two 25 series resistors R_{MUX} modelling the ADS1256-CN-M internal resistance. The signal measured when SDCS is enabled is equal to the total IR voltage drop:$I_{SDC} \times (2R_{MUX} + R_{SENS})$. Note that , when the sensor is directly short-circuited ($R_{SENS} = 0$). With SDCS enabled, the ADS1255/1256-CN-M will still measure a small signal: $I_{SDC} \times 2R_{MUX}$.

9.1.6 Oper/Short Sensor Detection

The sensor detect current sources (SDCS) provide a means to verify the integrity of the external sensor connected to the ADS1255/1256-CN-M. When enabled, the SDCS supply a current (I_{SDC}) of approximately 0.5µA , 2µA, or 10µA to the sensor through the input multiplexer.The SDCS bits in the ADCON register enable the SDCS and set the value of I_{SDC}.

When the SDCS are enabled, the ADS1255/1256-CN-M automatically turns on the analog input buffer regardless of the BUFEN bit setting. This is done to prevent the input circuitry from loading the SDCS. AIN_P must stay below 3V tobe within the absolute input range of the buffer. To ensure this condition is met, a 3V clamp will start sinking current from AIN_P to AGND if AIN_P exceeds 3V. Note that this clamp is activated only when the SDCS are enabled.

Figure 21 shows a simplified diagram of ADS1255/1256-CN-M input structure with the external sensor modeled as resistance R_{SENS} between two input pins. When the SDCS are enabled, they source I_{SDC} to the input pin connected to AIN_P and sink I_{SDC} from the input pin connected to AIN_N. The two 25Ω series resistors, R_{MUX}, model the ADS1255/1256-CN-M internal resistances. The signal measured with the SDCS enable equals the total IR drop: $I_{SDC} \times (2R_{MUX} + R_{SENS})$. Note that when the sensor is a direct short (that is, R_{SENS} = 0), there will still be a small signal measured by the ADS1255/1256-CN-M when the SDCS are enabled: $I_{SDC} \times 2R_{MUX}$.

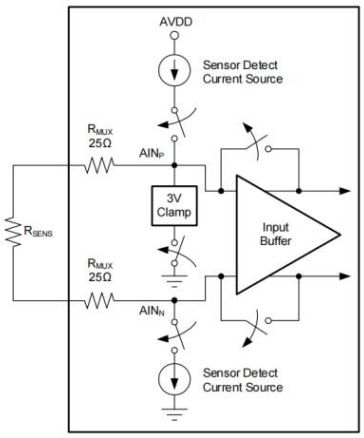


Figure 21 Sensor Detect Circuitry

NOTE: Arrows indicate switch positions when the SDCS are enabled.

9.1.7 Analog Input Buffer

To dramatically increase the input impedance presented by the ADS1255/1256-CN-M, the low-drift chopper-stabil -ized buffer can be enabled via the BUFEN bit in the STATUS register. The input impedance with the buffer enabled can be modeled by a resistor, as shown in Figure 22. Table 21 lists the values of Zeff for the different data rate settings.

The input impedance scales inversely with the frequency of CLKIN. For example, if f_{CLKIN} is reduced by half to 3.84MHz, Zeff for a data rate of 50SPS will double from 80MΩ to 160MΩ.

Figure 22 Effective Impedance With Buffer On

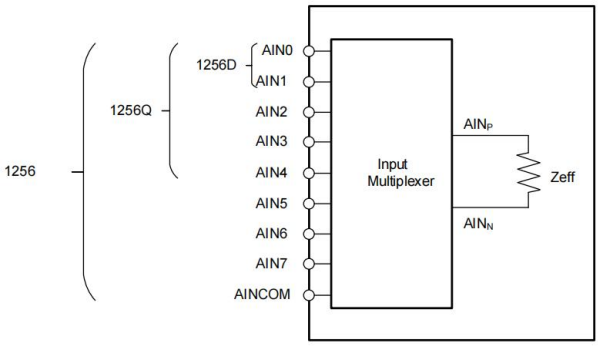


Table 21 Effective Impedance With Buffer On

Data Rate(SPS)	Zeff(MΩ)
60,000	17
30,000	17
15,000	17
7,500	17
3,750	17
2,000	17

1,000	34
500	68
100	68
60	68
≤50	80

NOTE: f_{CLK} = 7.68MHz.

With the buffer enabled, the voltage on the analog inputs with respect to ground (listed in the Electrical Characteristics as *Absolute Input Voltage*) must remain between AGND and AVDD – 2.0V. Exceeding this range reduces performance, in particular the linearity of the ADS1255/1256-CN-M. This same voltage range, AGND to AVDD – 2.0V, applies to the reference inputs when performing a self gain calibration with the buffer enabled.

9.1.8 Programmable Gain Amplifier (PGA)

The ADS1255/1256-CN-M is a very high resolution converter. To further complement its performance, the low-noise PGA provides even more resolution when measuring smaller input signals. For the best resolution, set the PGA to the highest possible setting. This will depend on the largest input signal to be measured. The ADS1255/1256-CN-M full-scale input voltage equals ±2V_{REF}/PGA. Table 22 shows the full-scale input voltage for the different PGA settings for V_{REF} = 2.5V. For example, if the largest signal to be measured is 1.0V, the optimum PGA setting would be 4, which gives a full-scale input voltage of 1.25V. Higher PGAs cannot be used since they cannot handle a 1.0V input signal.

Table 22 Full Scale Input Voltage vs. PGA Setting

PGA Setting	Full Scale Input Voltage V_{IN} (V_{REF}=2.5V)
1	±5V
2	±2.5V
4	±1.25V
8	±0.625V
16	±312.5mV
32	±156.25mV
64	±78.125mV
128	±39.0625mV

Note: The input voltage (V_{IN}) is the difference between the positive and negative inputs. Make sure neither input violates the absolute input voltage with respect to ground, as listed in the *Electrical Characteristics*.

The PGA is controlled by the ADCON register. Recalibrating the A/D converter after changing the PGA setting is recommended. The time required for self-calibration is dependent on the PGA setting. See the Calibration section for more details. The analog current and input impedance (when the buffer is disabled) vary as a function of PGA setting.

9.1.9 Modulator Input Circuitry

The ADS1255/1256-CN-M modulator measures the input signal using internal capacitors that are continuously charged and discharged. Figure 23 shows a simplified schematic of the ADS1255/1256-CN-M input circuitry with the input buffer disabled. Figure 24 shows the on/off timings of the switches of Figure 17. S1 switches close during the input sampling phase. With S1 closed, C_{A1} charges to AIN$_P$, C_{A2} charges to AIN$_N$, and C_B charges to (AIN$_P$ – AIN$_N$). For the discharge phase, S1 opens first and then S2 closes. C_{A1} and C_{A2} discharge to approximately AVDD/2 and C_B discharges to 0V. This two-phase sample/discharge cycle repeats with a period of τ_{SAMPLE}. This time is a function of the PGA setting as shown in Table 23 along with the values of the capacitor C_{A1} = C_{A2} = C_A and C_B.

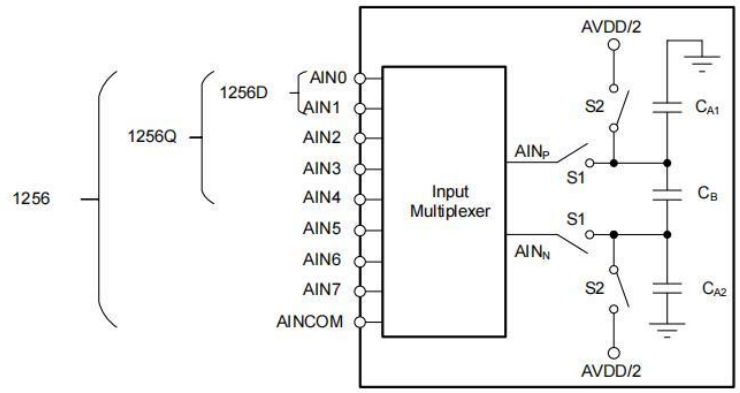


Figure 23 Simplified Input Structure With Buffer On

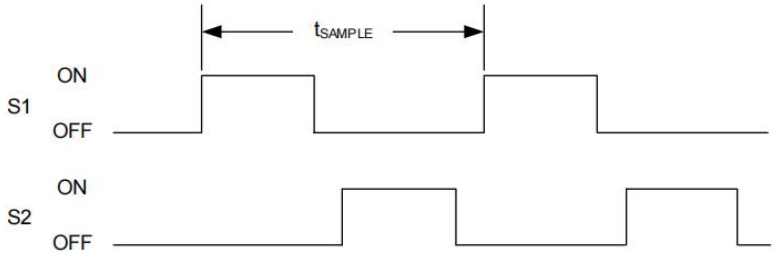


Figure 24 S1 and S2 Switch Timing for Figure 17

Table 23 Input Sampling Timet_{SAMPLE}, and CA and CB vs. PGA

PGA Setting	t_{SAMPLE}	C_A	C_B
1	f_{CLK}/4(521ns)	4.7pF	5.0pF
2	f_{CLK}/4(521ns)	8.4pF	9.0pF
4	f_{CLK}/4(521ns)	12pF	11pF
8	f_{CLK}/4(521ns)	19pF	21pF
16	f_{CLK}/4(521ns)	35pF	40pF
32	f_{CLK}/2(260ns)	33pF	37pF
64	f_{CLK}/2(260ns)	33pF	37pF
128	f_{CLK}/2(260ns)	33pF	37pF

Note: t_{SAMPLE} for f_{CLK} = 7.68MHz.

The charging of the input capacitors draws a transient current from the sensor driving the ADS1255/1256-CN-M inputs. The average value of this current can be used to calculate an effective impedance Zeff where Zeff = V_{IN} / $I_{AVERAGE}$. Figure 25 shows the input circuitry with the capacitors and switches of Figure 17 replaced by their effective impedances. These impedances scale inversely with the CLKIN frequency.

For example, if f_{CLKIN} is reduced by a factor of two, the impedances will double. They also change with the PGA setting. Table 24 lists the effective impedances with the buffer off for f_{CLKIN} = 7.68MHz.

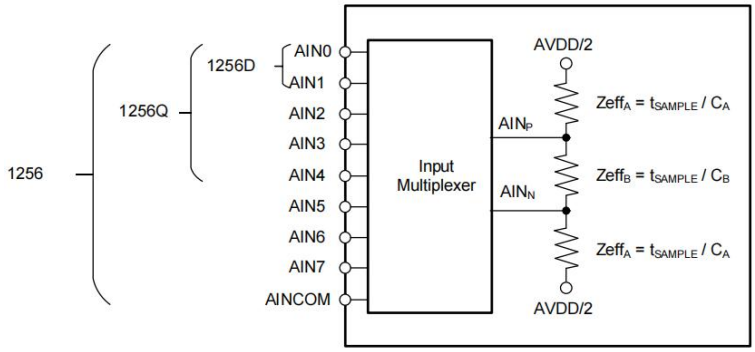


Figure 25 Analogue Input Effective Impedance With Buffer On

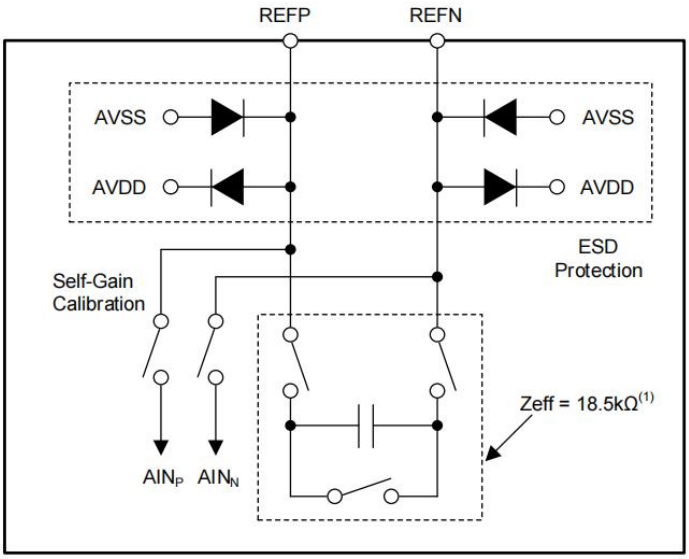
Table 24 Analogue Input Impedance With Buffer On

PGA 设置	$Zeff_A$(kΩ)	$Zeff_B$(kΩ)
1	110	105
2	62	58
4	45	47
8	27	25
16	15	13
32	8	7
64	8	7
128	8	7

Note: f_{CLK} = 7.68MHz.

9.1.10 Voltage Reference Input(VREFP、VREFN)

The voltage reference for the ADS1255/1256-CN-M A/D converter is the differential voltage between VREFP and VREFN:V_{REF} = VREFP – VREFN. The reference inputs use astructure similar to that of the analog inputs with thecircuitry on the reference inputs of Figure 26. The loadpresented by the switched capacitor can be modeled withan effective impedance (Zeff) of 15kΩ (Gain=1~32 data, impedance changes to 26k when Gain =64 or more).f_{CLKIN} = 7.68MHz.The temperature coefficient of theeffective impedance of the voltage reference inputs isapproximately 35ppm/°C.



(1) f_{CLK} = 7.68MHz

Figure 26 Simplified Reference Input Circuitry

ESD diodes protect the reference inputs. To keep these diodes from turning on, make sure the voltages on the reference pins do not go below AVSS by more than 100mV, and likewise do not exceed AVDD by 100mV:

$$-100mV < (VREFP \text{ or } VREFN) < AVDD + 100mV$$

During self gain calibration, all the switches in the input multiplexer are opened, VREFN is internally connected to AIN_N, and VREFP is connected to AIN_P. The input buffer may be disabled or enabled during calibration. When the buffer is disabled, the reference pins will be driving the circuitry shown in Figure 17 during self gain calibration, resulting in increased loading. To prevent this additional loading from introducing gain errors, make sure the circuitry driving the reference pins has adequate drive capability. When the buffer is enabled, the loading on the reference pins will be much less, but the buffer will limit the allowable voltage range on VREFP and VREFN during self or self gain calibration as the reference pins must remain within the specified input range of the buffer in order to establish proper gain calibration.

A high-quality reference voltage capable of driving the switched capacitor load presented by the ADS1255/1256-CN-M is essential for achieving the best performance. Noise and drift on the reference degrade overall system performance. It is especially critical that special care be given to the circuitry generating the reference voltages and their layout when operating in the low-noise settings (that is, with low data rates) to prevent the voltages reference from limiting performance.

9.1.11 Digital Filter

The programmable low-pass digital filter receives the modulator output and produces a high-resolution digital output. By adjusting the amount of filtering, trade offs can be made between resolution and data rate: filter more for higher resolution, filter less for higher data rate. The filter is comprised of two sections, a fixed filter followed by a programmable filter. Figure 27 shows the block diagram of the analog modulator and digital filter. Data is supplied to the filter from the analog modulator at a rate of $f_{CLKIN}/4$. The fixed filter is a 5th-order sinc filter with a decimation value of 64 that outputs data at a rate of $f_{CLKIN}/64$. The second stage of the filter is a programmable averager (1st-order sinc filter) with the number of averages set by the DRATE register. The data rate is a function of the number of averages (Num_Ave) and is given by Equation 5.

$$\text{Data Rate} = \left(\frac{f_{MOD}}{64}\right)\left(\frac{1}{\text{Num Ave}}\right) \quad (5)$$

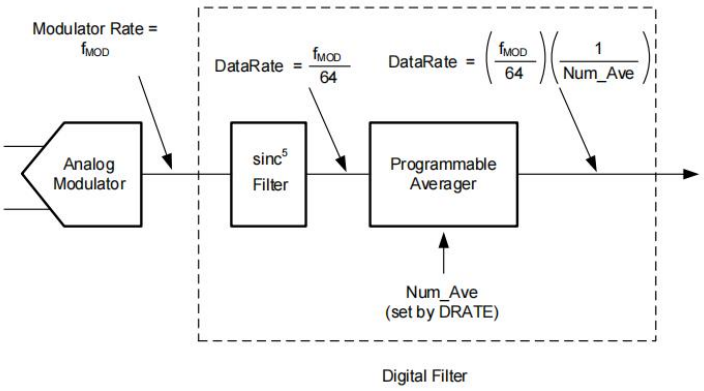


Figure 27 Block Diagram of the Analog Modulator and Digital Filter

Table 25 shows the averaging and corresponding data rate for each of the 16 valid DRATE register settings when f_{CLKIN} = 7.68MHz. Note that the data rate scales directly with the CLKIN frequency. For example, reducing f_{CLKIN} from 7.68MHz to 3.84MHz reduces the data rate for DR[7:0] = 11110000 from 30,000SPS to 15,000SPS.

Table 25 Number of Average and Data Rate for Each Valid DRATE Register Setting

DRATE[7:0]	Number of Average for Programmable Filter (Num_Ave)	Data Rate (SPS) (For f_{CLK} = 7.68MHz)
0000 0011 (03h)	12,000	2.5
0001 0011 (13h)	6000	5
0010 0011 (23h)	3000	10
0011 0011 (33h)	2000	15
0100 0011 (43h)	1200	25
0101 0011 (53h)	1000	30
0110 0011 (63h)	600	50
0111 0010 (72h)	500	60
1000 0010 (82h)	300	100
1001 0010 (92h)	60	500
1010 0001 (A1h)	30	1000
1011 0000 (B0h)	15	2000
1100 0000 (C0h)	8	3750
1101 0000 (D0h)	4	7500
1110 0000 (E0h)	2	15,000
1111 0000 (F0h)	1 (averager bypassed)	30,000

9.2 Frequency Response

The low-pass digital filter sets the overall frequency response for the ADS1255/1256-CN-M.The filter response is the product of the responses of the fixed and programmable filter sections and is given by Equation 6.

$$|H(f)| = |H_{sin^5}(f)| \times |H_{Averager}(f)| = \left| \frac{\sin\left(\frac{64\pi \times f}{f_{MOD}}\right)}{64 \times \sin\left(\frac{\pi \times f}{f_{MOD}}\right)} \right|^5 \times \left| \frac{\sin\left(\frac{64\pi \times Num\_Avef}{f_{MOD}}\right)}{Num\_Ave \times \sin\left(\frac{64\pi \times f}{f_{MOD}}\right)} \right| \quad (6)$$

The digital filter attenuates noise on the modulator output,including noise from within the ADS1255/1256-CN-M and external noise present on the ADS1255/1256-CN-M input signal. Adjusting the filtering by changing the number of averages used in the programmable filter changes the filter bandwidth. With a higher number of averages,bandwidth is reduced and more noise is attenuated.The low-pass filter has notches (or zeros) at the data output rate and multiples thereof. At these frequencies, the filter has zero gain. This feature can be useful when trying to eliminate a particular interference signal. For example,to eliminate 60Hz (and the harmonics) pickup, set the data rate equal to 2.5SPS, 5SPS,10SPS, 15SPS, 30SPS, or 60SPS. To help illustrate the filter characteristics,Figure 28 and Figure 29 show the responses at the data rate extremes of 30kSPS and 2.5SPS respectively.Table 26 summarizes the first-notch frequency and –3dB bandwidth for the different data rate settings.

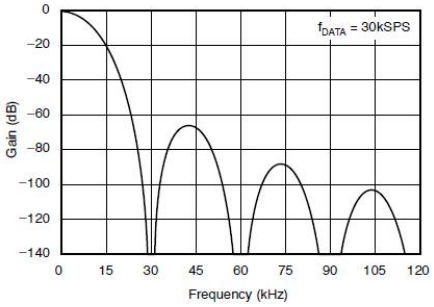


Figure 28 Frequency Response for Data Rate = 30kSPS

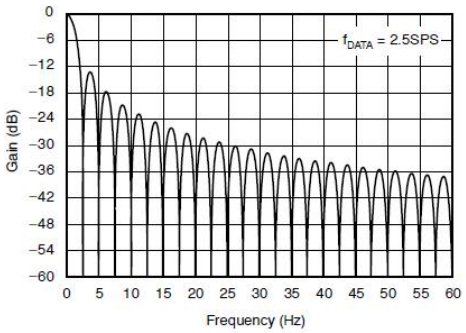


Figure 29 Frequency Response for Data Rate = 2.5kSPS

Table 26 First Trap and -3dB Filter Bandwidths

DATA RATE (SPS)		FIRST NOTCH (Hz)	–3dB BANDWIDTH (Hz)
30,000		30,000	6106
15,000		15,000	4807
7500		7500	3003
3750		3750	1615
2000		2000	878
1000		1000	441
500		500	221
100		100	44.2
60	Notch at 60Hz	60	26.5
50	Notch at 50Hz	50	22.1
30	Notch at 60Hz	30	13.3
25	Notch at 50Hz	25	11.1
15	Notch at 60Hz	15	6.63
10	Notch at 50Hz and 60Hz	10	4.42
5		5	2.21
2.5		2.5	1.1

Note: f_{CLK} = 7.68MHz.

The digital filter low-pass characteristic repeats at multiples of the modulator rate of fCLKIN/4. Figure 30 and Figure 31 show the responses plotted out to 7.68MHz at the data rate extremes of 30kSPS and 2.5 SPS. Notice how the responses near DC, 1.92MHz, 3.84MHz,5.76MHz, 7.68MHz, are the same. The digital filter will attenuate high-frequency noise on the ADS1255/1256-CN-M inputs up to the frequency where the response repeats. If significant noise on the inputs is present above this frequency, make sure to remove with external filtering.Fortunately, this can be done on the ADS1255/1256-CN-M with a simple RC filter, as shown in the *Applications* Section (see Figure 46).

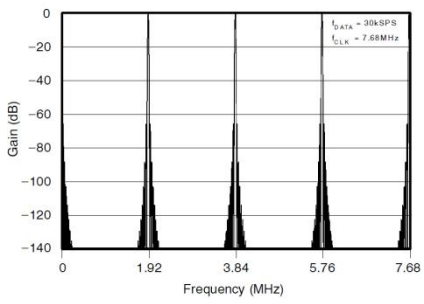


Figure 30 Frequency Response Output to 7.68MHz for Data Rate= 30kSPS

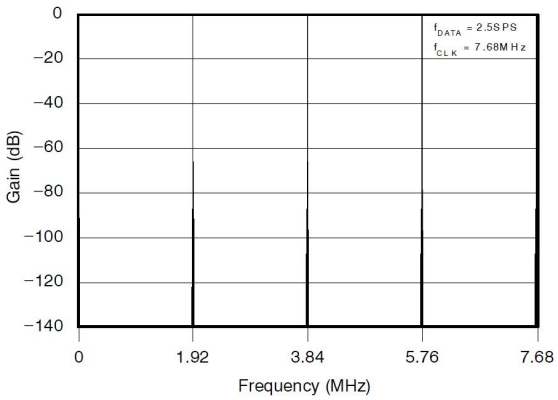


Figure 31 Frequency Response Output to 7.68MHz for Data Rate= 2.5kSPS

9.2.1 Settling Time

The ADS1255/1256-CN-M features a digital filter optimized for fast settling. The settling time (time required for a step change on the analog inputs to propagate through the filter) for the different data rates is shown in Table 27. The following sections highlight the single-cycle settling ability of the filter and show various ways to control the conversion process.

DATA RATE(SPS)	SETTLING TIME (t_{18}) (ms)
30,000	0.24
15,000	0.27
7500	0.34
3750	0.47
2000	0.7
1000	1.2
500	2.2
100	10.21
60	16.87
50	20.2
30	33.53
25	40.2
15	66.87
10	100.2
5	200.2
2.5	400.2

NOTE 1: f_{CLK} = 7.68MHz.

NOTE 2: One−shot mode requires a small additional delay to powerup the device from standby.

9.2.2 Settling Time Using Synchronisation

The SYNC/PDWN pin allows direct control of conversiontiming. Simply issue a Sync command or strobe the SYNC/PDWN pin after changing the analog inputs (see the Synchronization section for more information). The conversion begins when SYNC/PDWN is taken high,stopping the current conversion and restarting the digital filter. As soon as SYNC/PDWN goes low, the DRDY output goes high and remains high during the conversion.After the settling time (τ_{18}), DRDY goes low, indicating thatdata is available. The ADS1255/1256-CN-M settles in a singlecycle—there is no need to ignore or discard data aftersynchronization.Figure 32 showsthe data retrieval sequence following synchronization.

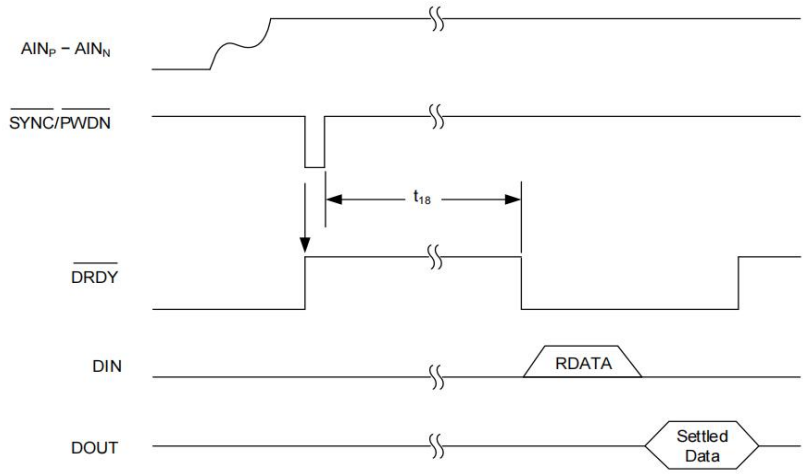


Figure 32 Data Retrieval After Synchronisation

9.2.3 Settling Time Using The Input Multiplexer

The most efficient way to cycle through the inputs is tochange the multiplexer setting (using a WREG commandto the multiplexer register MUX) immediately after DRDY goes low. Then, after changing the multiplexer, restart theconversion process by issuing the SYNC and WAKEUPcommands, and retrieve thedata with the RDATAcommand. Changing the multiplexer before reading thedata allows the ADS1256-CN-M to start measuring the new inputchannel sooner. Figure 33 demonstrates efficient inputcycling. There is no need to ignore or discard data whilecycling through the channels of the input multiplexerbecause the ADS1256-CN-M fully settles before DRDY goes low,indicating data is ready.

1. When DRDY goes low, indicating that data is readyfor retrieval, update the multiplexer register MUX using theWREG command. For example, setting MUX to 23h givesAINP = AIN2, AINN = AIN3.
2. Restart the conversion process by issuing a SYNCcommand immediately followed by a WAKEUP command.Make sure to follow timing specification t_{11} betweencommands.
3. Read the data from the previous conversion usingthe RDATA command.
4. When DRDY goes low again, repeat the cycle by first updating the multiplexer register, then reading thepreviousdata.

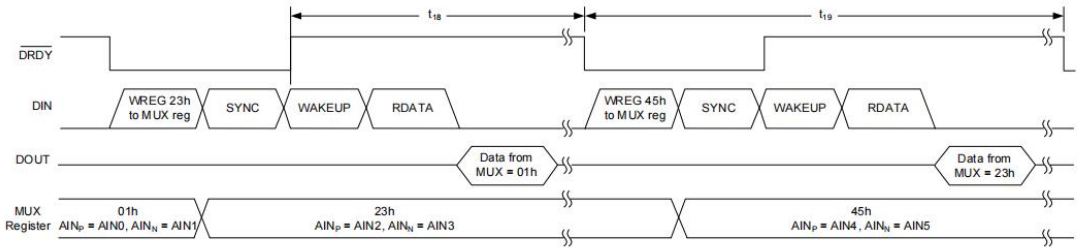


Figure 33 Cycling the ADS1256-CN-M Input Multiplexer

Table 28 gives the effective overall throughput ($1/t_{19}$) whencycling the input multiplexer. The values for throughput ($1/t_{19}$) assume the multiplexer was changed with a 3-byteWREG command and $f_{SCLK} = f_{CLKIN}/4$.

Table 28 Multiplexer Cycling Throughput

DATA RATE (SPS)	CYCLING THROUGHPUT ($1/t_{19}$) (Hz)
30,000	4374
15,000	3817
7500	3043
3750	2165
2000	1438
1000	837
500	456
100	98
60	59
50	50
30	30
25	25
15	15
10	10
5	5
2.5	2.5

NOTE: f_{CLK} = 7.68MHz.

9.2.4 Settling Time Using One-Shot Mode

A dramatic reduction in power consumption can be achieved in the ADS1255/1256-CN-M by performing one-shot conversions using the STANDBY command; the sequence for this is shown in Figure 20. Issue the WAKEUP command from Standby mode to begin a one-shot conversion. When using one–shot mode, an additional delay is required for the modulator to power up and settle. This delay may be up to 64 modulator clocks (64 x 4 x τCLKIN) or 33.3µs for a 7.68MHz master clock. Following the settling time (t_{18} + 256 x τCLKIN), DRDY will go low, indicating that the conversion is complete and data can be read using the RDATA command. The ADS1255/1256-CN-M settles in a single cycle—there is no need to ignore or discard data. When using one–shot mode, an addition al delay is required for the modulator to power up and settle. This delay may be up to 64 modulator clocks (64 x 4 x τCLKIN or 33.3µs for a 7.68MHz master clock. Following the data read cycle,issue another STANDBY comm and to reduce power consumption. When ready for the next measurement, repeat the cycle starting with another WAKEUP command.

9.2.5 Settling time While continuously Converting

After a synchronization, input multiplexer change, or wakeup from Standby mode,the ADS1255/1256-CN-M will continuously convert the analog input. The conversions coincide with the falling edge of DRDY. While contin -uously converting, it is often more convenient to consider settling times in terms of DRDY periods, as shown in Table 35.The DRDY period equals the inverse of the data rate.If there is a step change on the input sign- al while continuously converting, performing a synchronization operation to start a new conversion is reco -mmended.Otherwise, the next data will represent a combination of the previous and current input signal and should therefore be discarded. Figure 29 shows an example of readback in this situation.

Table 29 Data Settling Delay vs Data Rate

DATA RATE (SPS)	SETTLING TIME (DRDY Periods)
30,000	5
15,000	3

7500	2
3750	1
2000	1
1000	1
500	1
100	1
60	1
50	1
30	1
25	1
15	1
10	1
5	1
2.5	1

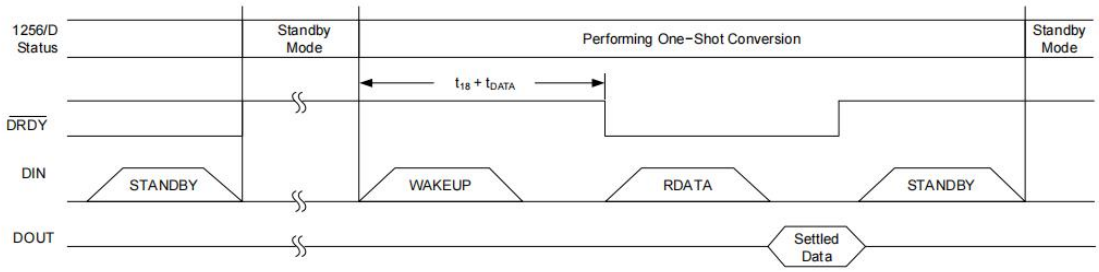


Figure 34 One-Shot Conversions Using the STANDBY Command

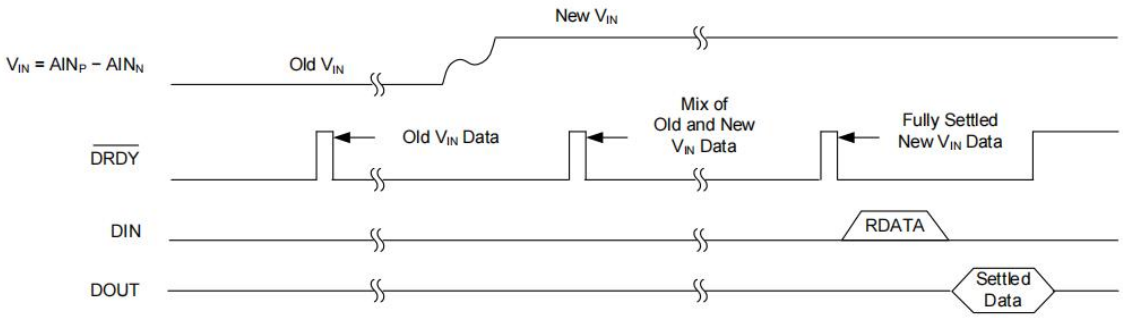


Figure 35 Step Change On VIN while Continuously Converting for Data Rate ≤ 3750SPS

9.2.6 Data Format

The ADS1255/1256-CN-M output 24 bits of data in Binary Two's Complement format. The LSB has a weight of $2V_{REF}/(PGA(2^{23} - 1))$. A positive full-scale input produces an output code of 7FFFFFh and the negative full-scale input produces an output code of 800000h. The output clips at these codes for signals exceeding full-scale. Table 30 summarizes the ideal output codes for different input signals.

Table 30 Ideal Output Codes vs Input Signal

INPUT SIGNAL $V_{IN}(AIN_P - AIN_N)$	IDEAL OUTPUT CODE
$\geq \frac{+2V_{REF}}{PGA}$	7FFFFFh
$\frac{+2V_{REF}}{PGA(2^{23}-1)}$	000001h
0	000000h
$\frac{-2V_{REF}}{PGA(2^{23}-1)}$	FFFFFFh
$\leq \frac{-2V_{REF}}{PGA}\left(\frac{2^{23}}{2^{23}-1}\right)$	800000h

Note: Excludes effects of noise, INL, offset, and gain errors.

9.3 General-Purpose Digital I/O (D0-D3)

The ADS1256-CN-M has 4 pins dedicated for digital I/O and the ADS1255-CN-M has 2 digital I/O pins. All of the digital I/O pins are individually configurable as either inputs or outputs through the IO register. The DIR bits of the IO register define whether each pin is an input or output, and the DIO bits control the status of the pins. Reading back the DIO register shows the state of the digital I/O pins, whether they are configured as inputs or outputs by the DIR bits. When digital I/O pins are configured as inputs, the DIO register is used to read the st ate of these pins. When configured as outputs, DIO sets the output value. On the ADS1255, the digital I/O pins D2 and D3 do not exist and the settings of the IO register bits that control operation of D2 and D3 have no eff ect on that device.

During Standby and Power-Down modes, the GPIO remain active. If configured as outputs, they continue to drive the pins. If configured as inputs, they must be driven (not left floating) to prevent excess power dissipation.The digital I/O pins are set as inputs after power-up or a reset, except for D0/CLKOUT, which is enabled as a clock output. If the digital I/O pins are not used, either leave them as inputs tied to ground or configure them as outputs. This prevents excess power dissipation.

9.3.1 Clock Output (D0/CLKOUT)

The clock output pin can be used to clock another device,such as a microcontroller. This clock can be configured to operate at frequencies of f_{CLKIN}, $f_{CLKIN}/2$, or $f_{CLKIN}/4$ using CLK1 and CLK0 in the ADCON register. Note that enabling the output clock and driving an external load will increase the digital power dissipation. Standby mode does not affect the clock output status. That is, if Standby is enabled, the clock output will continue to run during Standby mode. If the clock output function is not needed,it should be disabled by writing to the ADCON register after power-up or reset.

9.4 Clock Generation

The master clock source for the ADS1255/1256-CN-M can be provided using an external crystal or clock generator.When the clock is generated using a crystal, external capacitors must be provided to ensure start-up and a stable clock frequency, as shown in Figure 36. Any crystal should work with the ADS1255/1256-CN-M. Table 31 lists two crystals that have been verified to work. Long leads should be minimized with the crystal plac ed close to the ADS1255/1256-CN-M pins.

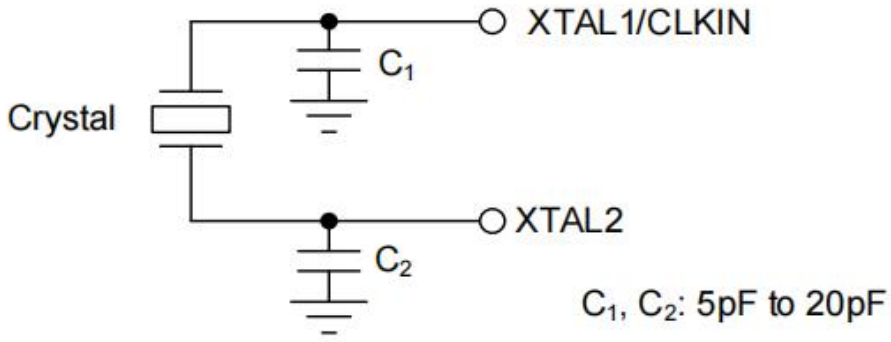


Figure 36 Crystal Connection

Table 31 Sample Crystals

MANUFACTURER	FREQUENCY	PART NUMBER
Citizen	7.68MHz	CIA/53383
ECS	8.0MHz	ECS-80-5-4

When using a crystal, neither the XTAL1/CLKIN nor XTAL2 pins can be used to drive any other logic. If other devices need a clock source, the D0/CLKOUT pin is available for this function. When using an external clock generator, supply the clock signal to XTAL1/CLKIN and leave XTAL2 floating. Make sure the external clock generator supplies a clean clock waveform. Overshoot and glitches on the clock will degrade overall performance.

9.5 Calibration

Offset and gain errors can be minimized using the ADS1255/1256-CN-M onboard calibration circuitry. Figure 37 shows the calibration block diagram. Offset errors are corrected with the Offset Calibration (OFC) register and, likewise, full-scale errors are corrected with the Full-Scale Calibration (FSC) register. Each of these registers is 24-bits and can be read from or written to.

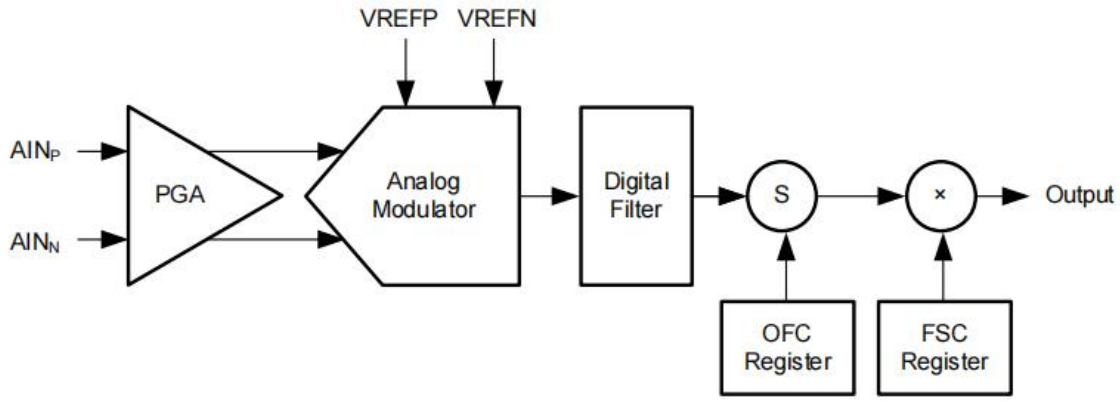


Figure 37 Calibration Block Diagram

The output of the ADS1255/1256-CN-M after calibration is shown in below. Where α and β vary with data rate settings shown in Table 32 along with the ideal values (assumes perfect analog performance) for OFC and FSC. OFC is a Binary Two's Complement number that can range from –8,388,608 to 8,388,607, while FSC is unipolar ranging from 0 to 16,777,215.

$$\text{Output} = \left(\frac{\text{PGA} \times V_{IN}}{2V_{REF}} - \frac{\text{OFC}}{\alpha}\right) \text{FSC} \times \beta$$

The ADS1255/1256-CN-M supports both self-calibration and system calibration for any PGA setting using a set of five commands: SELFOCAL, SELFGCAL, SELFCAL, SYSOCAL, and SYSGCAL. Calibration can be done at any time, though in many applications the ADS1255/1256-CN-M drift performance is low enough that a single calibration is all that is needed. $\overline{DRDY}$ goes high when calibration begins and remains so until settled data is ready afterwards.There is no need to discard data after a calibration. It is strongly recommended to issue a self-calibration command after power-up when the reference has stabilized. After a reset, the ADS1255/1256-CN-M performs self-calibration. Calibration must be performed whenever the data rate changes and should be performed when the buffer configuration or PGA changes.

Table 32 Calibration Values for Different Data Rate Settings

Data Rate (SPS)	α	β	Ideal OFC	Ideal FSC
30,000	400000H	1.8639	000000H	44AC08H
15,000	400000H	1.8639	000000H	44AC08H
7500	400000H	1.8639	000000H	44AC08H
3750	400000H	1.8639	000000H	44AC08H
2000	3C0000H	1.7474	000000H	494008H
1000	3C0000H	1.7474	000000H	494008H
500	3C0000H	1.7474	000000H	494008H
100	4B0000H	2.1843	000000H	3A99A0H
60	3E8000H	1.8202	000000H	4651F3H
50	4B0000H	2.1843	000000H	3A99A0H
30	3E8000H	1.8202	000000H	4651F3H
25	4B0000H	2.1843	000000H	3A99A0H
15	3E8000H	1.8202	000000H	4651F3H
10	5DC000H	2.7304	000000H	2EE14CH
5	5DC000H	2.7304	000000H	2EE14CH
2.5	5DC000H	2.7304	000000H	2EE14CH

8.5.1 Self-Calibration

Self-calibration corrects internal offset and gain errors.During self-calibration, the appropriate calibration signals are applied internally to the analog inputs.

SELFOCAL performs a self offset calibration. The analog inputs AIN_P and AIN_N are disconnected from the signal source and connected to AVDD/2. See Table 19 for the time required for self offset calibration for the different data rate settings. As with most of the ADS1255/1256-CN-M timings, the calibration time scales directly with f_{CLKIN}. Self offset calibration updates the OFC register.

Table 33 Self Offset and System Offset Calibration Timing

DATA RATE (SPS)	SELF OFFSET CALIBRATION AND SYSTEM OFFSET CALIBRATION TIME
30,000	446μs
15,000	512μs
7500	646μs
3750	912μs

2000	1.4ms
1000	2.4ms
500	4.4ms
100	20.4ms
60	33.7ms
50	40.4ms
30	67.1ms
25	80.4ms
15	133.7ms
10	200.4ms
5	400.5ms
2.5	800.4ms

NOTE: f_{CLK} = 7.68MHz

SELFGCAL performs a self gain calibration. The analog inputs AINP and AINN are disconnected from the signal source and AINP is connected internally to VREFP while AINN is connected to VREFN. Self gain calibration can be used with any PGA setting. However, in order to obtain the best gain error perform ance, it is recommended that a gain error correction be performed once when the programmable gain amplifier PGA is set to gain=1. When it is necessary to set the PGA to another gain, the gain error data from the PGA gain=1 can continue to be used.

Using the buffer will limit the common-mode range of the reference inputs during self gain calibration since they will be connected to the buffer inputs and must be within the specified analog input rang e. When the voltage on VREFP or VREFN exceeds the buffer analog input range (AVDD – 2.0V) , the buffer must be turned off during self gain calibration. Otherwise, use system gain calibration or write the gain coefficients directly to the FSC register.Table 34 shows the time required for self gain calibr- ation for the different data rate and PGA settings. Self gain calibration updates the FSC register.

Table 34 Self Gain Calibration Timing

Data Rate (SPS)	PGA Gain Setting				
	1	2	4	8	16, 32, 64
30,000	446μs	446μs	479μs	546μs	679μs
15,000	512μs	512μs	512μs	579μs	579μs
7500	646μs	646μs	647μs	648μs	779μs
3750	912μs				
2000	1.4ms				
1000	2.5ms				
500	4.5ms				
100	21.1ms				
60	34.1ms				
50	41.7ms				
30	67.9ms				
25	83.0ms				
15	135.3ms				
10	207.0ms				
5	413.8ms				
2.5	827.0ms				

NOTE: f_{CLK} = 7.68MHz

SELFCAL performs first a self offset and then a self gain calibration. The analog inputs are disconnected from the from the signal source during self-calibration. When using the input buffer with self-calibration, make sure to observe the common-mode range of the reference inputs as described above. Table 35 shows the time required for self-calibration for the different data rate settings.Self-calibration updates both the OFC and FSC registers.

Table 35 Self - Calibration Timing

Data Rate (SPS)	PGA Gain Setting				
	1	2	4	8	16, 32, 64
30,000	655μs	655μs	688μs	755μs	888μs
15,000	755μs	755μs	755μs	821μs	821μs
7500	955μs	955μs	955μs	955μs	1088μs
3750	1.4ms				
2000	2.1ms				
1000	3.6ms				
500	6.7ms				
100	31.2ms				
60	51.0ms				
50	61.9ms				
30	101.4ms				
25	123.2ms				
15	202.2ms				
10	307.2ms				
5	613.9ms				
2.5	1227.3ms				

9.5.2 System Calibration

System calibration corrects both internal and external offset and gain errors using the SYSOCAL and SYSGCAL commands. During system calibration, the appropriate calibration signals must be applied by the user to the inputs.

SYSOCAL performs a system offset calibration. The user must supply a zero input differential signal. The ADS1255/1256-CN-M then computes a value that will nullify the offset in the system. Table 36 shows the time required for system offset calibration for the different data rate settings.Note this timing is the same for the self offset calibration.System offset calibration updates the OFC register.

SYSGCAL performs a system gain calibration. The user must supply a full-scale input signal to the ADS1255/1256-CN-M.The ADS1255/1256-CN-M then computes a value to nullify the gain error in the system. System gain calibration can correct inputs that are 80% of the full-scale input voltage and larger. Make sure not to exceed the full-scale input voltage when using system gain calibration. Table 36 shows the time required for system gain calibration for the different data rate settings.System gain calibration updates the FSC register.

Table 36 System Gain Calibration Timing

Data Rate (SPS)	System Gain Calibration Time
30,000	417μs
15,000	484μs
7500	617μs
3750	884μs
2000	1.4ms
1000	2.4ms

500	4.4ms
100	20.4ms
60	33.7ms
50	40.4ms
30	67.0ms
25	80.4ms
15	133.7ms
10	200.4ms
5	400.4ms
2.5	800.4ms

Note: f_{CLK} = 7.68MHz

9.5.3 Auto-Calibration

Auto-calibration can be enabled (ACAL bit in STATUS register) to have the ADS1255/1256-CN-M automatically initiate a self-calibration at the completion of a write command (WREG) that changes the data rate, PGA setting, or Buffer status.

9.6 Serial Interface

The SPI-compatible serial interface consists of four signals: $\overline{CS}$, SCLK, DIN, and DOUT, and allows a controller to communicate with the ADS1255/1256-CN-M. The programmable functions are controlled using a set of on-chip registers. Data is written to and read from these registers via the serial interface. The DRDY output line is used as a status signal to indicate when a conversion has been completed. $\overline{DRDY}$ goes low when new data is available. Figure 3 shows the timing diagram for interfacing to the ADS1255/1256-CN-M.

9.7 Chip Selection ($\overline{CS}$)

The chip select ($\overline{CS}$) input allows individual selection of a ADS1255/1256-CN-M device when multiple devices share the serial bus. $\overline{CS}$ must remain low for the duration of the serial communication. When $\overline{CS}$ is taken high, the serial interface is reset and DOUT enters a high impedance state. $\overline{CS}$ may be permanently tied low.

9.8 Serial Clock (SCLK)

The serial clock (SCLK) features a Schmitt-triggered input and is used to clock data on the DIN and DOUT pins into and out of the ADS1255/1256-CN-M. Even though the input has hysteresis, it is recommended to keep SCLK as clean as possible to prevent glitches from accidentally shifting the data. If SCLK is held low for 32 $\overline{DRDY}$ periods, the serial interface will reset and the next SCLK pulse will start a new communication cycle. This time out feature can be used to recover communication when a serial interface transmis-sion is interrupted. A special pattern on SCLK will reset the chip; see the RESET section for more details on this procedure. When the serial interface is idle, hold SCLK low.

9.8.1 Data Input (DIN) And Data Output (DOUT)

The data input pin (DIN) is used along with SCLK to send data to the ADS1255/1256-CN-M. The data output pin (DOUT) along with SCLK is used to read data from the ADS1255/1256-CN-M. Data on DIN is shifted into the part on the falling edge of SCLK while data is shifted out on DOUT on the rising edge of SCLK. DOUT is high impedance when not in use to allow DIN and DOUT to be connected together and be driven by a bi-dir ectional bus.
Note: the RDATAC command must not be issued while DIN and DOUT are connected together.

9.8.2 Data Ready ($\overline{DRDY}$)

The $\overline{DRDY}$ output is used as a status signal to indicate when conversion data is ready to be read. $\overline{DRDY}$ goes low when new conversion data is available. It is reset high when all 24 bits have been read back using Read Data (RDATA) or Read Data Continuous (RDATAC) command. It also goes high when the new conversion data is being updated. Do not retrieve during this update period as the data is invalid. If data is not retrieved, DRDY will only be high during the update time as shown in Figure 38.

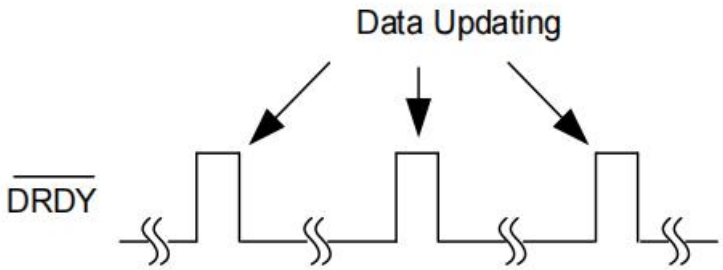


Figure 38 $\overline{\text{DRDY}}$ with No Data Retrieval

After changing the PGA, data rate, buffer status, writing to the OFC or FSC registers, and enabling or disabling the sensor detect circuitry, perform a synchronizationoperation to force $\overline{\text{DRDY}}$ high.It will stay high until valid data is ready. If auto-calibration is enabled (by setting the ACAL bit in the STATUS register) , $\overline{\text{DRDY}}$ will go low after the self-calibration is complete and new data are valid.Exiting from Reset, Synchronization, Standby or Power-Down mode will also force $\overline{\text{DRDY}}$ high. $\overline{\text{DRDY}}$ will go low as soon as valid data are ready.

9.8.3 Synchronisation

Synchronization of the ADS1255/1256-CN-M is available to coordinate the A/D conversion with an external event and also to speed settling after an instantaneous change on the analog inputs (see Conversion Time using Synchronization section).Synchronization can be achieved either using the $\overline{\text{SYNC}}$/$\overline{\text{PDWN}}$ pin or with the SYNC command. To use the $\overline{\text{SYNC}}$/ $\overline{\text{PDWN}}$ pin, take it low and then high, making sure to meet timing specification t_{16} and t_{16B}. Synchronization occurs after $\overline{\text{SYNC}}$/$\overline{\text{PDWN}}$ is taken high.No communication is possible on the serial interface while $\overline{\text{SYNC}}$/$\overline{\text{PDWN}}$ is low. If the $\overline{\text{SYNC}}$/$\overline{\text{PDWN}}$ pin is held low for 20 $\overline{\text{DRDY}}$ periods the ADS1255/1256-CN-M will enter Power-Down mode.To synchronize using the SYNC command, first shift in all eight bits of the SYNC command. This stops the operation of the ADS1255/1256-CN-M. When ready to synchr-onize, issue the WAKEUP command. Synchronization occurs on the first rising edge of the master clock after the first SCLK used to shift in the WAKEUP command. After a synchronization operation, either with the $\overline{\text{SYNC}}$/$\overline{\text{PDWN}}$ pin or the SYNC command, $\overline{\text{DRDY}}$ stays high until valid data is ready.

9.8.4 Standby Mode

The standby mode shuts down all of the analog circuitry and most of the digital features. The oscillator continues to run to allow for fast wakeup. If enabled, clock output D0/CLKOUT will also continue to run during during Standbymode. To enter Standby mode, issue the STANDBY command. To exit Standby mode, issue the WAKEUP command.$\overline{\text{DRDY}}$ will stay high after exiting Standby mode until valid data is ready. Standby mode can be used to perform one-shot conversions; see Settling Time Using One-Shot Mode section for more details.

9.8.5 Power-Down Mode

Holding the $\overline{\text{SYNC}}$/$\overline{\text{PDWN}}$ pin low for 20 $\overline{\text{DRDY}}$ cycles activates the Power-Down mode. During Power-Down mode, all circuitry is disabled including the oscillator and the clock output.To exit Power-Down mode, take the $\overline{\text{SYNC}}$/$\overline{\text{PDWN}}$ pin high. Upon exiting from Power-Down mode, the ADS1255/1256-CN-M crystal oscillator typically requires 30ms to wake up. If using an external clock source, 8192 CLKIN cycles are needed before conversions begin.

9.8.6 Reset

There are three methods to reset the ADS1255/1256-CN-M: the $\overline{\text{RESET}}$ input pin, RESET command, and a special SCLK reset pattern.

When using the $\overline{\text{RESET}}$ pin, take it low to force a reset. Make sure to follow the minimum pulse width timing specifications before taking the $\overline{\text{RESET}}$ pin back high.

The $\overline{\text{RESET}}$ command takes effect after all eight bits have been shifted into DIN. Afterwards, the reset releases automatically.

The ADS1255/1256-CN-M can also be reset with a special pattern on SCLK (see Figure4). Reset occurs on the falling edge of the last SCLK edge in the pattern. After performing the operation, the reset releases automatically.

On reset, the configuration registers are initialized to their default state except for the CLK0 and CLK1 bits in the ADCON register that control the D0/CLKOUT pin. These bits are only initialized to the default state when $\overline{\text{RESET}}$ is performed using the $\overline{\text{RESET}}$ pin. After releasing from $\overline{\text{RESET}}$, self-calibration is performed, regardless of the reset method or the state of the ACAL bit before $\overline{\text{RESET}}$.

9.8.7 Power up

All of the configuration registers are initialized to their default state at power-up. A self-calibration is then performed automatically. For the best performance, it is strongly recommended to perform an additional self-calibration by issuing the SELFCAL command after the power supplies and voltage reference have had time to settle to their final values.

10. REGISTER MAP

The operation of the ADS1255/1256-CN-M is controlled through a set of registers. Collectively, the registers contain all the information needed to configure the part, such as data rate, multiplexer settings, PGA setting, calibration, etc., and are listed in Table 37.

Table 37 Register Map

Address	Register	Reset Value	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
00h	STATUS	x1h	ID[3:0]				ORDER	ACAL	BUFEN	$\overline{\text{DRDY}}$
01h	MUX	01h	PSEL[3:0]				NSEL[3:0]			
02h	ADCON	20h	0	CLK[1:0]		SDCS[1:0]		PGA[2:0]		
03h	DRATE	F0h	DR[7:0]							
04h	IO	E0h	DIR[3:0]				DIO[3:0]			
05h	OFC0	00h	OFC[7:0]							
06h	OFC1	00h	OFC[15:8]							
07h	OFC2	00h	OFC[23:16]							
08h	FSC0	08h	FSC[7:0]							
09h	FSC1	ACh	FSC[15:8]							
0Ah	FSC2	44h	FSC[23:16]							
0Bh	CFG0	00h	REJ50_60[1:0]		DAISY_EN	0	REG_CHK	MODE[2:0]		
0Ch	CFG1	00h	INTGPIO[1:0]		IOSC_SLO W	-	LP_GLOAB L	IOSC_FSEL[1:0]		PARITYE N
0Dh	CFG2	22h	MODDIV[2:0]			CLKDIV[2:0]			CLKMON	CLKSRC
0Eh	CFG3	05h	DELAY[2:0]			POWERMODE[1:0]		XOSCRN G	XOSCLP	-
0Fh	CFG4	00h	SPITO[1:0]		CRC_EN[1:0]		CHKSUM	START	RNG_EN[1:0]	

10h	CFG5	00h	TEMP_EN	0	COMBUF_E N	COMSW_ EN	PRECHGLP	SHORTP_ EN	IO_SR	IO_HD
11h	DEV_CFG	00h	VCMBUFL P	VCMDI VLP	-	PRECHG_ EN	INBUFLP	CAP_HAL F	INT234O TALP	-
12h	MOD_ST AT	00h	RNG_ERR	CRC_E RR	DAISY	CLK_FAUL T	REG_MDF	SHORTH	SHORTL	PARITY
13h	DEV_STA T	04h	RES_MISS	EF_UE RR	EF_CERR	RESET[1:0]		WAKEUP	0	SPILOCK
14h	CMD_ST AT	00h	0	0	0	0	CMDSTAT[3:0]			

10.1 STATUS：StatUs Register (Address 00h)

Reset value = x1h , return to the summary table.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
ID3	ID2	ID1	ID0	ORDER	ACAL	BUFEN	DRDY

Table 38 STATUS Register Description

Bit	Field	Description
7：4	ID3，ID2，ID1，ID0	Factory-programmed identification bits (read-only) ID[3]: 0 = Register map space 00h-0Fh 1 = Register map space 00h-0Ah ID[2:0]: Pinout 000 = Six or eight analog channels; no XOSC. 001 = 1255 010 = 1256 100-111 = Reserved
3	ORDER	Data Output Bit Order 0 = most significant bit first (default) 1 = least significant bit first
2	ACAL	Auto Calibration 0=Autocalibration disabled (default) 1=Autocalibration enabled When auto-calibration is enabled, auto-calibration begins after completion of the WREG command to change the PGA (bits 0-2 of the adcon register) DR (bits 7-0 in the DRATE register) or BUFEN (bit 1 in the status register) values.
1	BUFEN	Analogue input buffer enabled 0=Buffer disabled (default) 1=Buffer enabled
0	DRDY	Data Ready (read-only) This bit replicates the state of the DRDY pin.

10.2 MUX： Input MultipleXer Control Register (Address 01H)

Reset value = 01h , return to the summary table.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
PSEL3	PSEL2	PSEL1	PSEL0	NSEL3	NSEL2	NSEL1	NSEL0

Table 39 MUX Register Description

Bit	Field	Description
7:4	PSEL3, PSEL2, PSEL1, PSEL0	Positive input channel (AINP) select 0000 = AIN0 (default) 0001 = AIN1 0010 = AIN2 (1256 only) 0011 = AIN3 (1256 only) 0100 = AIN4 (1256 only) 0101 = AIN5 (1256 only) 0110 = AIN6 (1256 only) 0111 = AIN7 (1256 only) When ID3 is 1 (register address 00-0Ah): 1xxx = AINCOM (when PSEL3 = 1, PSEL2, PSEL1, PSEL0 are “don’t care”.) When ID3 is 0 (register address 00-0Fh): 1000-1010 = AINCOM 1011 = Temperature sensor 1100 = (AVDD – AVSS)/4 1101 = (DVDD – DGND)/4 1110 = Open 1111 = VCOM ((AVDD + AVSS)/2)
3:0	NSEL3, NSEL2, NSEL1, NSEL0	Negative input channel (AINN) select 0000 = AIN0 0001 = AIN1 (default) 0010 = AIN2 (1256 only) 0011 = AIN3 (1256only) 0100 = AIN4 (1256 only) 0101 = AIN5 (1256 only) 0110 = AIN6 (1256 only) 0111 = AIN7 (1256 only) 1xxx = AINCOM (when NSEL3 = 1, NSEL2, NSEL1, NSEL0 are “don’t care”.)

NOTE: When using an ADS1255-CN-M make sure to only select the available inputs.

10.3 ADCON： A/D Control Register (Address 02H)

Reset value = 20h , return to the summary table.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	CLK1	CLK0	SDCS1	SDCS0	PGA2	PGA1	PGA0

Table 40 ADCON Register Description

Bit	Field	Description
7	0	Reserved, always 0 (read only)

6:5	CLK1, CLK0	D0/CLKOUT clock out rate setting 00 = Clock Out OFF 01 = Clock Out Frequency = fCLK (default; do not change to other setting in daisy chain mode) 10 = Clock Out Frequency = fCLK/2 (fCLK after CLKDIV) 11 = Clock Out Frequency = fCLK/4 (fCLK after CLKDIV) When not using CLKOUT, it is recommended that it be turned off. These bits can only be reset using the RESET pin.
4:3	SDCS1, SCDS0	Sensor detect current sources 00 = Sensor Detect OFF (default) 01 = Sensor Detect Current = 0.5µA 10 = Sensor Detect Current = 2µA 11 = Sensor Detect Current = 10µA The Sensor Detect Current Sources can be activated to verify the integrity of an external sensor supplying a signal to the 1256/1255. A shorted sensor produces a very small signal while an open-circuit sensor produces a very large signal.
2:0	PGA2, PGA1, PGA0	Programmable gain amplifier setting 000 = 1 (default) 001 = 2 010 = 4 011 = 8 100 = 16 101 = 32 110 = 64 111 = 128

10.4 DRATE： A/D Data Rate (Address 03H)

Reset value = F0h , return to the summary table.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DR7	DR6	DR5	DR4	DR3	DR2	DR1	DR0

The 16 valid Data Rate settings are shown below. Make sure to select a valid setting as the invalid settings may produce unpredictable results.

Table 41 DRATE Register Description

Bit	Field	Description
7:0	DR[7: 0]	Data rate setting 11110000 = 30,000SPS (default) 11100000 = 15,000SPS 11010000 = 7,500SPS 11000000 = 3,750SPS 10110000 = 2,000SPS 10100001 = 1,000SPS 10010010 = 500SPS 10000010 = 100SPS 01110010 = 60SPS 01100011 = 50SPS 01010011 = 30SPS 01000011 = 25SPS 00110011 = 15SPS 00100011 = 10SPS 00010011 = 5SPS 00000011 = 2.5SPS

NOTE: for f_{CLK} = 7.68MHz. Data rates scale linearly with f_{CLK}.

10.5 I/O： GPIO Control Register (Address 04H)

Reset value = E0h , return to the summary table.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DIR3	DIR2	DIR1	DIR0	DIO3	DIO2	DIO1	DIO0

The states of these bits control the operation of the general-purpose digital I/O pins. The ADS1256-CN-M has 4 I/O pins: D3, D2 , D1,and D0/CLKOUT. The ADS1255-CN-M has two digital I/O pins: D1 and D0/CLKOUT. When using an ADS1255-CN-M, the register bits DIR3, DIR2, DIO3, and DIO2 can be read from and written to but have no effect.

Table 42 I/O Register Description

Bit	Field	Description
7	DIR3	Digital I/O direction for digital I/O pin D3 (used on 1256 only) 0 = D3 is an output. 1 = D3 is an input (default).
6	DIR2	Digital I/O direction for digital I/O pin D2 (used on 1256 only) 0 = D2 is an output. 1 = D2 is an input (default).
5	DIR1	Digital I/O direction for digital I/O pin D1 0 = D1 is an output. 1 = D1 is an input (default).
4	DIR0	Digital I/O direction for digital I/O pin D0/CLKOUT 0 = D0/CLKOUT is an output (default). 1 = D0/CLKOUT is an input.
3:0	DI0[3:0]	Status of digital I/O pins D3, D2, D1, D0/CLKOUT Reading these bits will show the state of the corresponding digital I/O pin, whether if the pin is configured as an input or output by DIR3-DIR0. When the digital I/O pin is configured as an output by the DIR bit, writing to the corresponding DIO bit will set the output state. When the digital I/O pin is configured as an input by the DIR bit, writing to the corresponding DIO bit will have no effect. When DO/CLKOUT is configured as an output and CLKOUT is enabled (using CLK1, CLK0 bits in the ADCON register), writing to DIO0 will have no effect.

10.6 OFC0： Offset Calibration Byte 0, least significant byte (Address 05H)

Reset value depends on calibration results. Return to summary table.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OFC07	OFC06	OFC05	OFC04	OFC03	OFC02	OFC01	OFC00

10.7 OFC1： Offset Calibration Byte 1 (Address 06H)

Reset value depends on calibration results. Return to summary table.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OFC15	OFC14	OFC13	OFC12	OFC11	OFC10	OFC09	OFC08

10.8 OFC2： Offset Calibration Byte 2, most significant byte (Address 07H)

Reset value depends on calibration results. Return to summary table.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
OFC23	OFC22	OFC21	OFC20	OFC19	OFC18	OFC17	OFC16

10.9 FSC0： Full-scale Calibration Byte 0, least significant byte (Address 08H)

Reset value depends on calibration results. Return to summary table.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FSC07	FSC06	FSC05	FSC04	FSC03	FSC02	FSC01	FSC00

10.10 FSC1： Full-scale Calibration Byte 1 (Address 09H)

Reset value depends on calibration results. Return to summary table.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FSC15	FSC14	FSC13	FSC12	FSC11	FSC10	FSC09	FSC08

10.11 FSC2： Full-scale Calibration Byte 2, most significant byte (Address 0AH)

Reset value depends on calibration results. Return to summary table.

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
FSC23	FSC22	FSC21	FSC20	FSC19	FSC18	FSC17	FSC16

10.12 CFG0（Address 0BH）

Reset value = 00h , return to the summary table.

Table 43 CFG0 Register Description

Bit	Field	Type	Reset	Description
7:6	REJ50_60[1:0]	R/W	00b	50Hz and 60Hz noise rejection When REJ50_60 is not zero, if DR = 92h (500SPS), the internal system will automatically adjust the data rate to 250Hz. For other DR settings, to reach 250Hz, CLKDIV/MODDIV should be configured—MODDIV = 6 when DR = B0h (2000SPS) or CLKDIV = 2 when DR = A1h (1000SPS). 0: No 50Hz or 60Hz rejection 1: Simultaneous 50Hz and 60Hz rejection 2: 50Hz rejection only 3: 60Hz rejection only
5	DAISY_EN	R	0b	Allow Daisy Chain mode 0: No daisy chain available 1: Enable daisy chain mode
4	0	R	0b	Reserved
3	REG_CHK	R/W	0b	Enable register integrity checker REG_MDF = 1 if registers have been modified. 0: No effect 1: Enable register integrity checker

2:0	MODE[2:0]	R/W	000b	Operation mode 0: Continuous conversion mode 1: Single conversion mode 2: Standby mode 3: Two steps to power down: Step 1: Must write 3 to MODE[2:0] (even it is already 3). Step 2: Pull $\overline{SYNC}/\overline{PWDN}$ low. (Pulling $\overline{SYNC}/\overline{PWDN}$ high to exit). 4: Internal offset calibration 5: Internal gain calibration 6: System offset calibration 7: System gain calibration

10.13 CFG1（Address 0CH）

Reset value = 00h , return to the summary table

Table 44 CFG1 Register Description

Bit	Field	Type	Reset	Description
7:6	INTGPIO[1:0]	R/W	00b	Interrupt output to D0/D1 pin, including clock fault (INT1) and ADC out of range (INT2) 0: D0/D1 normal 1: INT1 and INT2 output to D0 2: INT1 and INT2 output to D1 3: INT1 output to D0, and INT2 output to D1
5	IOSC_SLOW	R/W	0b	Internal OSC frequency selection 0: 8MHz 1: 4MHz
4	-	R/W	0b	Reserved
3	LP_GLOBAL	R/W	0b	Chip works in low power mode. 0: Normal 1: Low power mode
2:1	IOSC_FSEL[1:0]	R/W	00b	Internal OSC frequency divider 0: Divided by 1 1: Divided by 2 2: Divided by 4 3: Divided by 8
0	PARITYEN	R/W	0b	Enable parity bit 0: No effect 1: PARITY bit enabled

10.14 CFG2（Address 0DH）

Reset value = 22h , return to the summary table

Table 45 CFG2 Register Description

Bit	Field	Type	Reset	Description
7:5	MODDIV[2:0]	R/W	01b	Modulation CLK divider after system clock 0: Divided by 2 (data rate double, maximum 60kSPS.) 1: Divided by 4 (default) 2: Divided by 6 3: Divided by 8 4: Divided by 12 5: Divided by 16 6: Divided by 32 7: Divided by 40
4:2	CLKDIV[2:0]	R/W	000b	Divide the selected clock source to generate the system clock ($t_{CLK} = 1/f_{CLK}$) 0: Divided by 1 1: Divided by 2 2: Divided by 4 3: Divided by 8 4: Divided by 16 5: Divided by 32 6: Divided by 64 7: Divided by 128
1	CLKMON	R/W	1b	Clock source monitor 0: No clock monitor 1: If the selected clock source (CLKIN/XTAL) is stopped, set XOSC_F and switch to internal OSC. After clock source recovers, it will switch back.
0	CLKSRC	R/W	0b	Clock source selection 0: CLKIN/XTAL for 1256/1255, XTAL for others Enable XOSC for 1255 when ID[1:0] = 01 or for 1256 when ID[1:0] = 10 1: Internal clock (controlled by IOSC_SLOW, IOSC_FSEL) To save power, writing CLKSRC = 0 twice will disable internal clock if CLKMON = 0; writing CLKSRC = 1 twice will disable XOSC. To enable again, need to wait more time.

10.15 CFG3（Address 0EH）

Reset value = 01h , return to the summary table

Table 46 CFG3 Register Description

Bit	Field	Type	Reset	Description
7:5	DELAY[2:0]	R/W	000b	Programmable delay before each conversion start It can increase the low duration of the $\overline{DRDY}$ pin. 0: No delay 1: 1 × 64 × t_{MOD} (33.3μs) 2: 4 × 64 × t_{MOD} (0.13ms) 3: 10 × 64 × t_{MOD} (0.33ms) 4: 25 × 64 × t_{MOD} (0.83ms) 5: 50 × 64 × t_{MOD} (1.67ms) 6: 125 × 64 × t_{MOD} (4.1ms) 7: 250 × 64 × t_{MOD} (8.3ms) Data in () is at f_{CLK} = 7.68MHz.
4:3	POWERMODE[1:0]	R/W	00b	Low power control for analog part 0: ~7mA (typical) 1: ~4mA (typical) 2: ~1.7mA (typical) 3: > 10mA (typical)
2	XOSCRNG	R/W	1b	XOSC frequency range 0: High frequency range (1~16MHz) 1: Low frequency range (4~8MHz)
1	XOSCLP	R/W	0b	XOSC low power mode 0: XOSC normal mode with directly CLKIN function 1: XOSC enters low power mode with amplitude loop control.
0	Reserved	R/W	1b	Reserved

10.16 CFG4（Address 0FH）

Reset value = 00h , return to the summary table

Table 47 CFG4 Register Description

Bit	Field	Type	Reset	Description
7:6	SPITO[1:0]	R/W	00b	SPI timeout reset (SPI interface only) 0: Disabled (default) 1: Timeout reset when SCLK is inactive for 256 t_{CLK}. 2: Timeout reset when SCLK is inactive for 1024 t_{CLK}. 3: Timeout reset when SCLK is inactive for 4096 t_{CLK}.
5:4	CRC_EN[1:0]	R/W	00b	Enable CRC check during register write/read and conversion data read 0: No CRC 1: Register read/write using byte XOR checksum 2: CRC checksum enabled ($X^8 + X^2 + X^1 + 1$) 3: CRC checksum enabled ($X^4 + X^1 + 1$)

3	CHKSUM	R/W	0b	Checksum. When CRC_EN is 2 or 3, only 24-bit conversion data are used for calculation. 0: Disabled (default) 1: Conversion data checksum byte included in readback
2	START	R/W	0b	Writing 1 to this bit triggers start conversion. 0: No effect 1: Writing 1 starts a new conversion.
1:0	RNG_EN[1:0]	R/W	00b	ADC out of range detection (enable MOD_STAT[7] and INT2) 0: No effect 1: Set RNG_ERR when input reaches VREF. 2: Set RNG_ERR when input reaches VREF / 2. 3: Set RNG_ERR when input reaches VREF × 2.

10.17 CFG5（Address 10H）

Reset value = 00h , return to the summary table

Table 48 CFG5 Register Description

Bit	Field	Type	Reset	Description
7	TEMP EN	R/W	0b	Temperature sensor enable 0: Disable 1: Enable
6	0	R	0b	
5	ALLCOMBUF_EN	R/W	0b	Power switch configuration (set AINCOM to VCMBUF) 0: Switch is always open (default). 1: Enable AINCOM drive out; disable in power-down mode
4	ALLCOMSW_EN	R/W	0b	Power switch configuration (set AINCOM to AVSS) 0: Switch is always open (default). 1: Switch is automatically closed during conversion and opened in power- down mode.
3	PRECHGLP	R/W	0b	Buffer pre-charge low power selection 0: High power 1: Low power
2	SHORT_PROT_EN	R/W	0b	IO (D0~3, $\overline{\text{DRDY}}$, DOUT) output shorted to enable VDD/VSS protection 0: Disable 1: When IO is shorted to VDD/VSS, it will lower the drive strength for protection.
1	IO_SR	R/W	0b	IO (D0~3, $\overline{\text{DRDY}}$, DOUT) output slew rate 0: Disable 1: Enable slew rate
0	IO_HD	R/W	0b	IO (D0~3, $\overline{\text{DRDY}}$, DOUT) output high drive 0: Disable 1: Enable IO high drive

10.18 DEV_CFG（Address 11H）

Reset value = 00h , return to the summary table

Table 47 DEV CFG Register Description

Bit	Field	Type	Reset	Description
7	VCMBUFLP	R/W	0b	VCM low power selection 0: High power 1: Low power
6	VCMDIVLP	R/W	0b	VCM divider low power selection 0: High power 1: Low power
5	LSBUFLP	R/W	0b	Low-side buffer low power selection 0: High power 1: Low power
4	PRECHG_EN	R/W	0b	PGA precharge enable (clear it when MODDIV = 0 and CLKDIV = 0) 0: Disable 1: Enable
3	INBUFLP	R/W	0b	Input buffer low power selection 0: High power 1: Low power
2	CAP_HALF	R/W	0b	Internal capacitor reduced half 0: No effect 1: Reduced half
1	INT234OTALP	R/W	0b	Modulator integrator OTA2/3/4 low power selection 0: High power 1: Low power
0	-	R/W	0b	Reserved

10.19 MOD_STAT（Address 12H）

Reset value = 00h , return to the summary table

Table 48 MOD STAT Register Description

Bit	Field	Type	Reset	Description
7	RNG_ERR	R	0b	Overrange or underrange has occurred. 0: No error happens. 1: Voltage is out of range. The error flag will output to the D1/D0 pin if INTGPIO is set.
6	CRC_ERR	R	0b	It sets when the CRC value accompanying a write operation does not correspond with the information sent. It is reset after being read. 0: No error happens. 1: CRC error happens.
5	DAISY	R	0b	Daisy Chain mode 0: Not Daisy Chain mode 1: Daisy Chain mode

4	CLK_FAULT	R	0b	Clock fault happens. It resets when there is no clock monitor or clock source is back to normal. 0: No fault happens. 1: Selected CLKIN/XTAL clock fault occurs, and the clock source switches to internal OSC.
3	REG_MDF	R/W	0b	Indicates that registers have been modified by command/reset (SCLK pattern/RESET command) if REG_CHK = 1. 0: No register modification 1: Registers have been modified. Write 0 to clear the modification.
2	SHORTH	R	0b	D0-D3/DRDY/DOUT pin shorted to VDD 0: Not shorted 1: Shorted
1	SHORTL	R	0b	D0-D3/DRDY/DOUT pin shorted to ground 0: Not shorted 1: Shorted
0	PARITY	R	0b	Parity check of the conversion result 0: Even number of 1s in the conversion data 1: Odd number of 1s in the conversion data

10.20 DEV_STAT（Address 13H）

Reset value = 04h , return to the summary table

Table 49 DEV STAT Register Description

Bit	Field	Type	Reset	Description
7	RES_MISS	R	0b	Conversion result overwritten 0: Normal 1: Conversion result is overwritten.
6	EF_UERR	R	0b	eFuse uncorrectable error happens. 0: No error happens. 1: Error happens. The error will be sent to D0 if CLK[1:0] = 1.
5	EF_CERR	R	0b	eFuse correctable error happens. 0: No error happens. 1: Error happens.
4:3	RESET[1:0]	R	0b	What reset happened last time. 0: Power-on/pin reset happens. 1: RESET command happens. 2: SCLK pattern reset happen. 3: Reserved
2	WAKEUP	R	1b	Device in wakeup or standby mode 0: Standby mode 1: Wakeup mode
1	0	R	0b	Reserved

SELFGCAL	Gain Self-Calibration	1111	0010	(F2h)	
SYSOCAL	System Offset Calibration	1111	0011	(F3h)	
SYSGCAL	System Gain Calibration	1111	0100	(F4h)	
SYNC	Synchronize the A/D Conversion	1111	1100	(FCh)	
STANDBY	Begin Standby Mode	1111	1101	(FDh)	
RESET	Reset to Power-Up Values	1111	1110	(FEh)	
WAKEUP/NOP	Completes SYNC and Exits Standby Mode, and clock out data	1111	1111	(FFh)	
RREG1	Read from REG r rrrr	100r	rrrr	(8xh,9xh)	000n nnnn
WREG1	Write to REG r rrrr	011r	rrrr	(6xh,7xh)	000n nnnn
LOCK	Lock to prevent registers write and commands (except NOP/RREG/RREG1/UNLOCK)	1110	0010	(E2h)	
UNLOCK	Unlock the LOCK command	1110	0101	(E5h)	
CIDSET	Set sequential numbers to daisy-chain devices as ID, r rrrr to 1st one	101r	Rrrr	(Axh,Bxh)	
CIDOP	Send followed 1 command to matched ID (r rrrr) daisy-chain device	110r	Rrrr	(E0h,E1h)	
CALLOP	Send followed 1 command to all daisy-chain devices	1110	000r	(E0h,E1h)	

NOTE 1: n = number of registers to be read/written - 1. For example, to read/write three registers, set nnnn = 2 (0010).
NOTE 2: r = start register address for read/write commands

11.1 RDATA：Read Data

Issue this command after $\overline{DRDY}$ goes low to read a single conversion result. After all 24 bits have been shifted out on DOUT, $\overline{DRDY}$ goes high. It is not necessary to read back all 24 bits, but $\overline{DRDY}$ will then not return high until new data is being updated. See the Timing Characteristics for the required delay between the end of the RDATA command and the beginning of shifting data on DOUT: t_6.

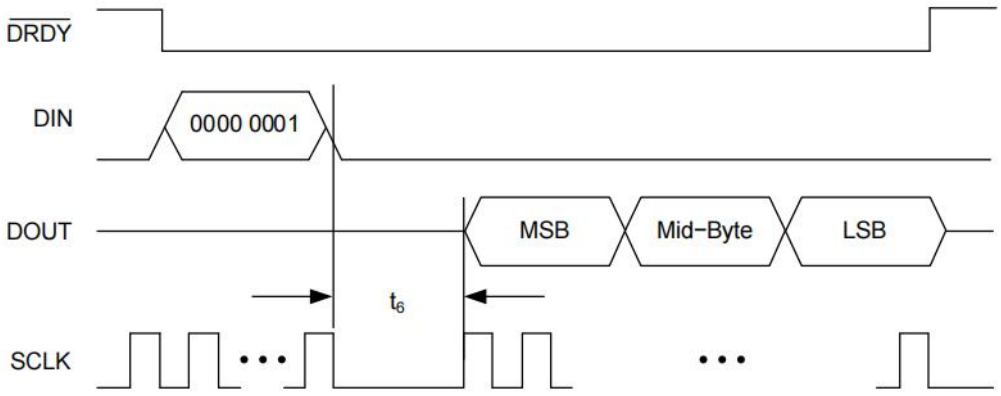


Figure 39 RDATA Command Sequence

11.2 RDATAC: Read Data Continuous

Description: Issue command after $\overline{DRDY}$ goes low to enter the Read Data Continuous mode. This mode enables the continuous output of new data on each $\overline{DRDY}$ without the need to issue subsequent read commands. After all 24 bits have been read, $\overline{DRDY}$ goes high. It is not necessary to read back all 24 bits, but $\overline{DRDY}$ will then not return high until new data is being updated. This mode may be terminated by the Stop Read Data Continuous command (SDATAC). Because DIN is constantly being monitored during the Read Data Continuous mode for the SDATAC or RESET command, do not use this mode if DIN and DOUT are connected together. See the Timing Characteristics for the required delay between the end of the RDATAC command and the beginning of shifting data on DOUT: t_6.

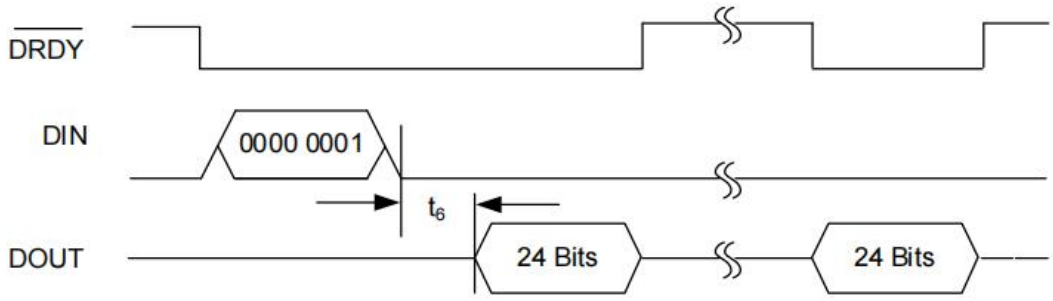


Figure 40 RDATAC Command Sequence

On the following $\overline{DRDY}$, shift out data by applying SCLKs. The Read Data Continuous mode terminates if input_data equals the SDATAC or RESET command in any of the three bytes on DIN.

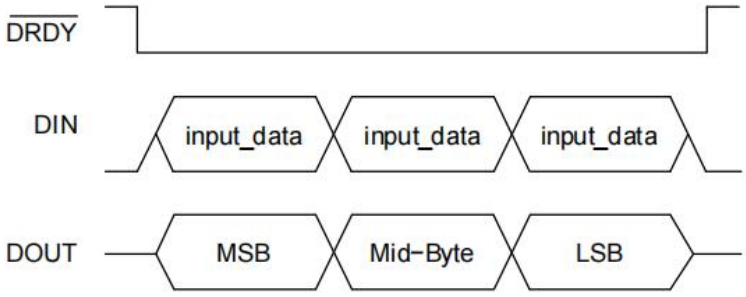


Figure 41 DIN And DOUT Command Sequence During Read Continuous Mode

11.3 SDATAC: Stop Read Data Continuous

Description: Ends the continuous data output mode. (see RDATAC). The command must be issued after $\overline{DRDY}$ goes low and completed before $\overline{DRDY}$ goes high.

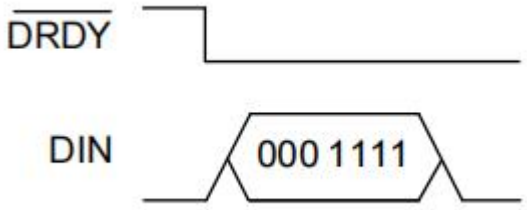


Figure 42 SDATAC Command Sequence

11.4 RREG: Read from Registers

Output the data from up to 11 registers starting with the register address specified as part of the command.The number of registers read will be one plus the second byte of the command. If the count exceeds the remaining registers,the addresses will wrap back to the beginning.

1st Command Byte: 0001 *rrrr* where *rrrr* is the address of the first register to read.
2nd Command Byte: 0000 *nnnn* where *nnnn* is the number of bytes to read – 1. See the Timing Characteristics for the required delay between the end of the RREG command and the beginning of shifting data on DOUT: t_6.

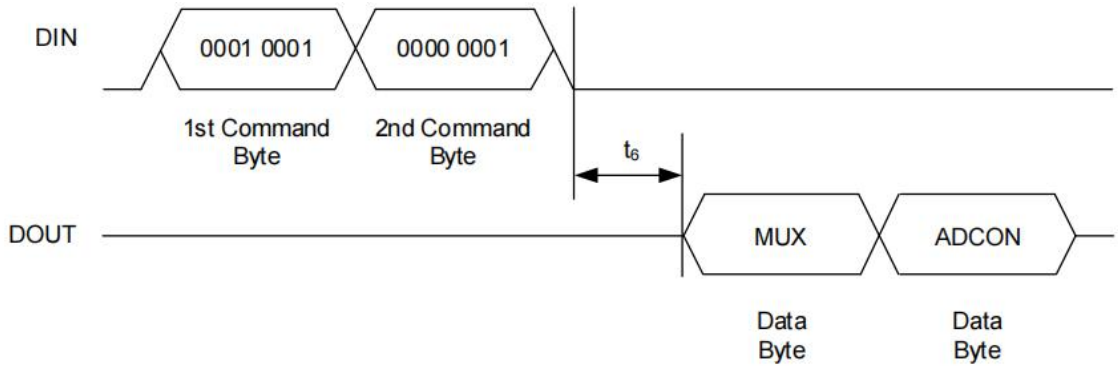


Figure 43 RREG Command Example: Read Two Registers Starting from Register 01h (multiplexer)

11.5 WREG: Write to Registers

Write to the registers starting with the register specified as part of the command. The number of registers that will be writte is one plus the value of the second byte in the command.

1st Command Byte: 0101 *rrrr* where *rrrr* is the address to the first register to be written.

2nd Command Byte: 0000 *nnnn* where *nnnn* is the number of bytes to be written – 1.

Data Byte(s): data to be written to the registers.

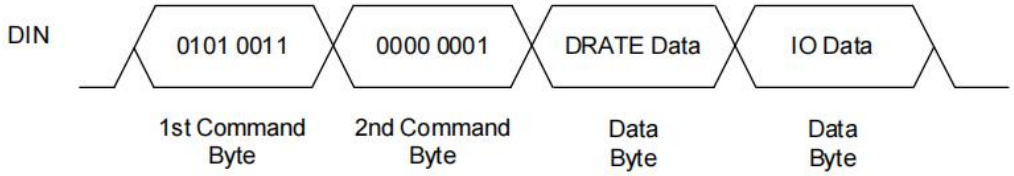


Figure 44 WREG Command Example: Write Two Registers Starting from 03h (DRATE)

11.6 SELFCAL：Self Offset and Gain Calibration

Description: Performs a self offset and self gain calibration. The Offset Calibration Register (OFC) and Full-Scale Calibration Register (FSC) are updated after this operation. $\overline{\text{DRDY}}$ goes high at the beginning of the calibration. It goes low after the calibration completes and settled data is ready. Do not send additional commands after issuing this command until $\overline{\text{DRDY}}$ goes low indicating that the calibration is complete.

11.7 Autofocusing：Self Offset Calibration

Description: Performs a self offset calibration. The Offset Calibration Register (OFC) is updated after this operation. $\overline{\text{DRDY}}$ goes high at the beginning of the calibration. It goes low after the calibration completes and settled data is ready. Do not send additional commands after issuing this command until $\overline{\text{DRDY}}$ goes low indicating that the calibration is complete.

11.8 SELFGCAL：Self Gain Calibration

Description: Performs a self gain calibration. The Full-Scale Calibration Register (FSC) is updated with new values after this operation. $\overline{\text{DRDY}}$ goes high at the beginning of the calibration. It goes low after the calibration completes and settled data is ready. Do not send additional commands after issuing this command until $\overline{\text{DRDY}}$ goes low indicating that the calibration is complete.

11.9 SYSOCAL： System Offset Calibration

Description: Performs a system offset calibration. The Offset Calibration Register (OFC) is updated after this operation. $\overline{DRDY}$ goes high at the beginning of the calibration. It goes low after the calibration completes and settled data is ready. Do not send additional commands after issuing this command until $\overline{DRDY}$ goes low indicating that the calibration is complete.

11.10 SYSGCAL： System Gain Calibration

Description: Performs a system gain calibration. The Full-Scale Calibration Register (FSC) is updated after this operation. $\overline{DRDY}$ goes high at the beginning of the calibration. It goes low after the calibration completes and settled data is ready. Do not send additional commands after issuing this command until $\overline{DRDY}$ goes low indicating that the calibration is complete.

11.11 SYNC： Synchronise the A/D Conversion

Description: This command synchronizes the A/D conversion. To use, first shift in the command. Then shift in the WAKEUP command. Synchronization occurs on the first CLKIN rising edge after the first SCLK used to shift in the WAKEUP command.

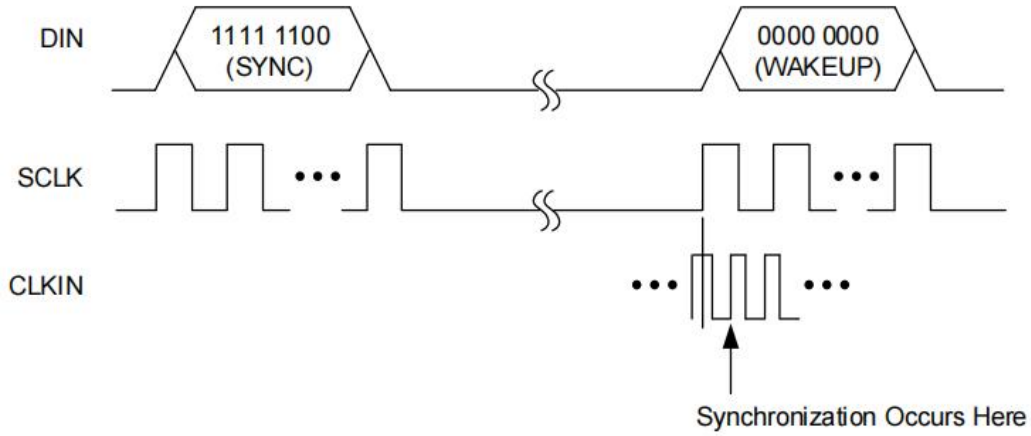


Figure 45 SYNC Command Sequence

11.12 STANDBY: Standby Mode/One-Shot Mode

Description: This command puts the ADS1255/1256-CN-M into a low-power Standby mode. After issuing the STANDBY command,make sure there is no more activity on SCLK while $\overline{CS}$ is low, as this will interrupt Standby mode. If $\overline{CS}$ is high, SCLK activity is allowed during Standby mode. To exit Standby mode, issue the WAKEUP command. This command can also be used to perform single conversions (see One-Shot Mode section) .

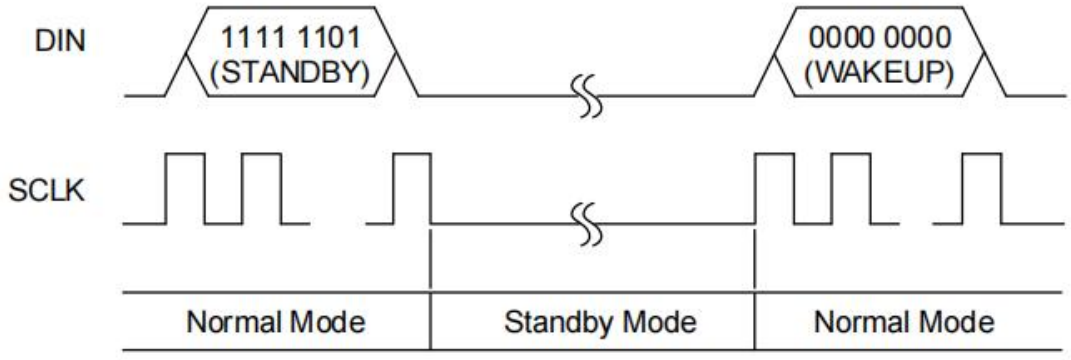


Figure 46 STANDBY Command Sequence

11.13 WAKEUP: Complete Synchronisation or EXit Standby Mode

Description: Used in conjunction with the SYNC and STANDBY commands. Two values (all zeros or all ones) are available for this command.

11.14 RESET: Reset Registers to Default Values

Description: Returns all registers except the CLK0 and CLK1 bits in the ADCON register to their default values. This command will also stop the Read Continuous mode: in this case, issue the RESET command after $\overline{DRDY}$ goes low.

11.15 Daisy Chain Model

Common Connections：SCLK、SYNC_PWDN、$\overline{CS}$

Serial Connection: DIN, DOUT (DIN of the next device).

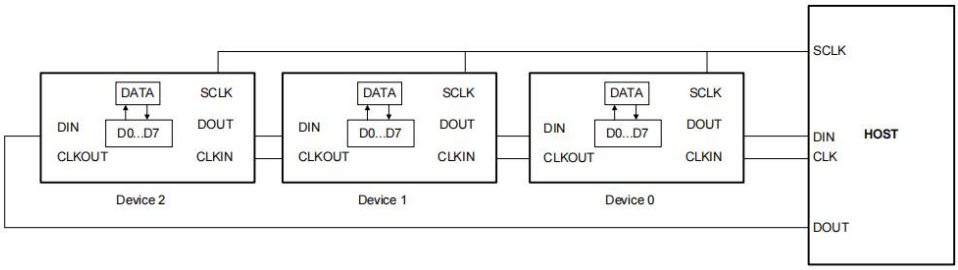


Figure 47 Serial Connection

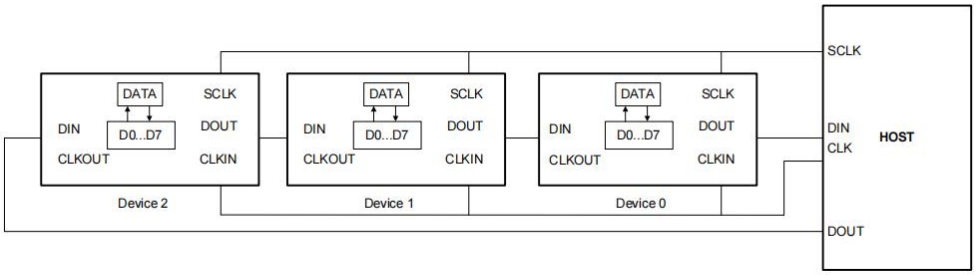


Figure 48 Serial or Common Connection

For DIN and DOUT, see Figure 47 and Figure 48 for serial connections.

For CLKIN/CLKOUT, see Figure 47 for serial connections and Figure 48 for common connections.

Figure 49 shows the Daisy Chain Mode Timing and SCLK Reset Timing. To enter daisy-chain mode, use the sequence shown in this figure.

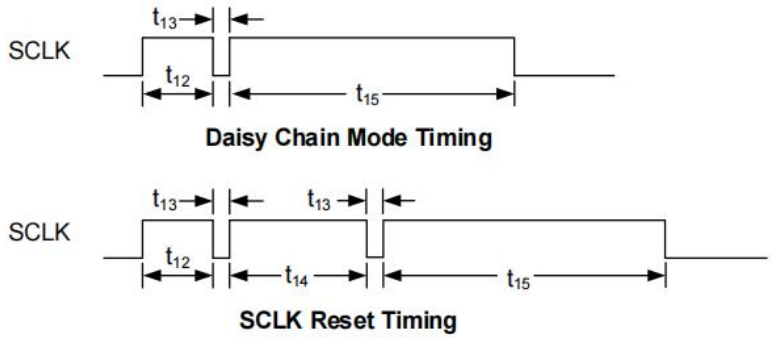


Figure 49 Daisy Chain Mode and SCLK Reset Timing

Table 52 lists the timing characteristics of Figure 49.

Table 52 Timing Characteristics for Figure 49

Parameter	Symbol	Min	Max	Units

SCLK Reset Pattern, First High Pulse	t_{12}	300	500	t_{CLK}(1)
SCLK Reset Pattern, Low Pulse	t_{13}	5		t_{CLK}
SCLK Reset Pattern, Second High Pulse	t_{14}	550	750	t_{CLK}
SCLK Reset Pattern, Third High Pulse	t_{15}	1050	1250	t_{CLK}

Note: Master clock period: $t_{CLK} = 1 / f_{CLK}$

To exit daisy chain mode, perform the following steps:

1. Turn on. _____
2. Pull the $\overline{RESET}$ pin low
3. Enter power-down mode.

11.15.1 Other Precautions

- The DOUT pin no longer outputs a high resistance state.
- Chained devices should have the same settings on DR/CRC/CLOCK.
- Pulling $\overline{CS}$ high will not only reset the SPI, it will also bypass DIN directly to DOUT. this operation will check daisy-chain connectivity or bypass some faulty/normal devices for efficiency.
- After the command 'CALLOP+CIDSET', the serial number (starting from CIDSET[4:0]; after 31, it is 0) is set as the device ID; later, 'CIDOP+CIDSET' only changes the ID of one device.
- After the 'RREG/RDATA/RDATAC' command, the result will be delayed 1 byte more than the normal mode. Note that t_6.
- After the 'RDATAC' command, the device will not accept new commands, including 'SDATAC', until $\overline{CS}$ \ pulse.There must be 24 or 32 (CRC_EN=1, 2 and CHSUM=1) SCLK pulses per $\overline{DRDY}$ falling edge.
- CRC-4 is not supported, and multibyte writing using CRC and 'CALLOP+RDATA(C)/RREG(1)' is not supported.
- After the 'CALLOP+STANDBY' command, use the all 1 'WAKUP/NOP' (FFh) command to wake up.

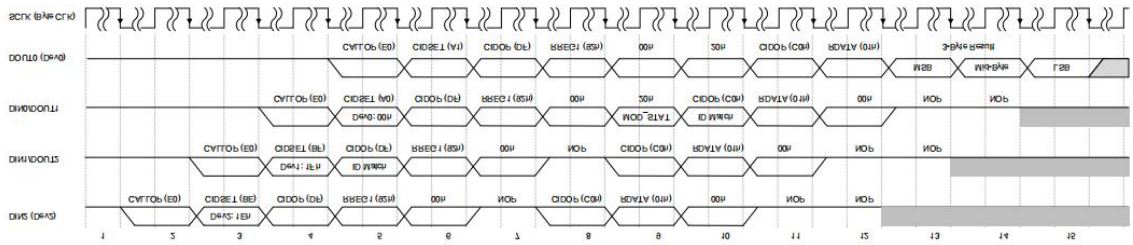


Figure 50 Sequence Diagram of Daisy Chain (Dev0-2)

11.15.2 CRC Computation In Daisy Chain Mode

For register writing, use "0101rrrr/011rrrrr + 0000 0000 + data".

For register reading, use"0001rrrr/100rrrrr + 000nnnnn + data".

11.15.3 CRC

CRC-4 provides a 4-bit CRC，CRC-8 provides an 8-bit CRC.When CRC_EN = 2 , Polynomial：$X^8+ X^2+ X^1 + 1$. for example:

1.Write OFC0 = 5Ah [successful only with CRC = 65h (CRC-8 of 0x55005a)]; Otherwise set CRC_ERR.

DIN =55005A65h).

2.Read OFC0 (CRC = e3h， DIN = 55000000h， DOUT = 5AE3h).

When CRC_EN = 2 , Polynomial：$X^4+ X^1+ 1$. for example :

1.Write OFC0 = EAh [Success with CRC = 70h (CRC-4 of 0x5500ea is 0x7)]； Otherwise set CRC_ERR.

DIN =5500EA70h).

2.Read OFC0 (CRC = e3h， DIN = 55000000h， DOUT = EA90h).

When CRC_EN = 1 , The byte is XOR.

1.Read OFC0 = 0x1C (CRC = 15h^1Ch = 09h， DIN = 15000000h， DOUT = 1C09h).

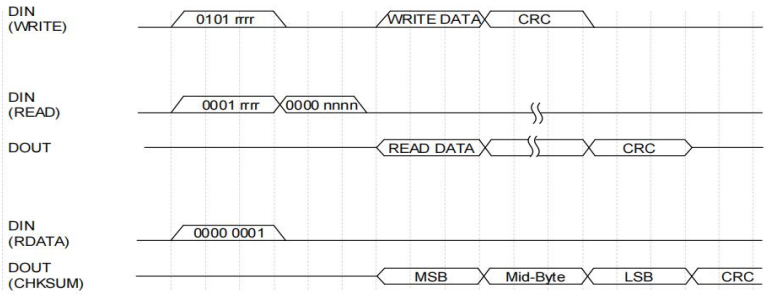


Figure 51 CRC

When CHKSUM=1, the RDATA/RDATAC command outputs the CRC value after the result. The following list shows the general procedure for calculating the CRC value. Assume that the shift register is n bits wide, where n is the number of CRC bits:

1.Set the polynomial value to 0x3 for 4-bit CRC and 0x07 for 8-bit CRC.

2.Set the shift register to all zeros.

3.Start with the MSB in the data stream. For every n bits:

- Align the MSB of the data stream with the MSB of the shift register. XOR the data with the shift register and store the result in the shift register.

- Test the highest bit of the shift register n times, performing one of the following operations each time:

•If the most significant bit(MSB) of the shift register is set, left-shift the register by one bit, XOR the result with the polynominal, and store the final result back into the shiftt register.

• If the highest valid bit of the shift register is not set, the register is shifted one bit to the left.

4.The result in the shift register is the CRC checksum value.For example,the CRC-8 of 654321h is 86h.

12. APPLICATIONS AND REALISATION

NOTE: The information contained in the application section below is not part of the Company's component specification and the Company does not warrant its accuracy or completeness. It is the responsibility of Company's customers to determine the suitability of components for their purposes. Customers should verify and test their design implementation to confirm system functionality.

12.1 Application Precautions

•When MODDIV[2:0] = 0 or 2 is set， Scaling the 30kSPS data rate to 60kSPS or 20kSPS.

•When IOSC is available and CLKMON = 1 , the chip can still operate without an external clock.When using a low-speed external clock(< 260kHz) or low-power standby mode,CLKMON must first be cleared to zero.The ADS1255/1256-CN-M can set CFG2[4:2] to > 5 (take care to ensure that $t_{SCLK} > 2.5\ t_{CLK}$)or stop the external clock before standby mode to reduce current.

•If the ADS1255/1256-CN-M uses only a crystal instead of an externally potted clock, CFG3[1] can be set to =1 to reduce the current.

•The CLK cycle can be 2.5 cycles of CLKIN, but it is guaranteed by design (not test).During the RDATAC state, SCLK can be faster (<20MHz) if only the NOP command is sent to DIN.

•If EF_UERR=1 and CLK=1, the CLKOUT pin will output high.

•For minimum dynamic power consumption, set LP_GLOBAL = 1、CAP_HALF = 1、POWERMODE[1:0] = 0b10、DEV_CFG = 0xff、CLKMON = 0，and set the clock speed and DVDD/AVDD as low as possible.

•To get the best gain error when PGA is not 0, calibrate the offset and save the OFC value at PGA=0. Adjust the PGA and write to the OFC using the saved values, then calibrate the gain.

12.2 Application Information

The ADS1256-CN-M and ADS1255-CN-M are very high resolution A/D converters.Getting the best performance from them requires careful attention to their support circuitry and printed circuit board (PCB) design.Figure 52 shows the basic connections of the ADS1255-CN-M.It is recommended that a single ground plane be used for both analogue and digital power supplies. This ground plane should be shared with the bypass capacitors and the analogue regulation circuits.However, avoid using this ground plane for noisy digital components such as microprocessors.If the separate grounding layer is used with the ADS1255/1256-CN-M, make sure that the analogue and digital layers are connected together.There should be no voltage difference between the ADS1255/1256-CN-M analogue and digital ground pins (AVSS and DGND).

As with any precision circuit, use good power bypass techniques.Smaller values of ceramic capacitors work well in parallel with larger values of tantalum capacitors or larger values of low-voltage ceramic capacitors.Place capacitors (especially ceramic capacitors) near the power supply pins.Run digital logic at the lowest possible voltage.This helps to reduce coupling to analogue inputs.Avoid ringing on digital inputs.Small resistors (≈100Ω) in series with the digital pins help control the alignment impedance.When $\overline{\text{RESET}}$ or SYNC/PWDN inputs are not used, connect directly to the ADS1255/1256-CN-M, DVDD pins.

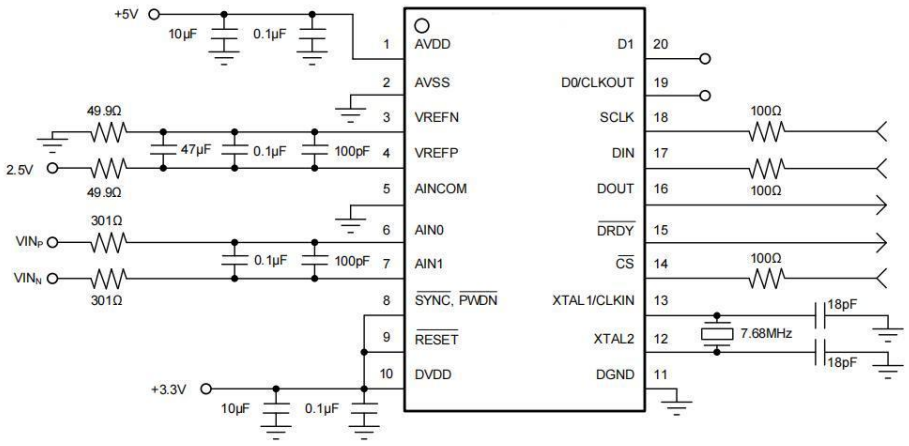


Figure 52 ADS1255-CN-M Basic Connection

Pay special attention to the reference and analogue inputs. These are the most critical circuits.At the voltage reference input, a low equivalent series resistance (ESR) capacitor is used for bypass.Make these capacitors as large as possible to maximise reference filtering.The ADS1255/1256-CN-M offer outstanding performance, and the voltage references can easily limit the overall performance if not selected properly.When using a standalone reference, make sure that it has very low noise, very low drift, and is capable of driving the ADS1255/1256-CN-M reference inputs.For voltage references (e.g., high output impedance references or resistive dividers) that are not suitable for directly driving the ADS1255/1256-CN-M, use the recommended buffer circuit shown in Figure 47.Ratiometric measurements where the input signal and reference track each other are slightly less sensitive, but verify that the reference signal is clean.

Typically, only a simple RC filter is required at the input (shown in Figure 53).This circuit limits high-frequency noise near the modulator frequency, see the Frequency Response section.Avoid using low grade dielectrics for capacitors to minimise temperature variations and leakage.Keep input alignments as short as possible and place components close to input pins. When using the ADS1256-CN-M, make sure to filter all input channels in use.

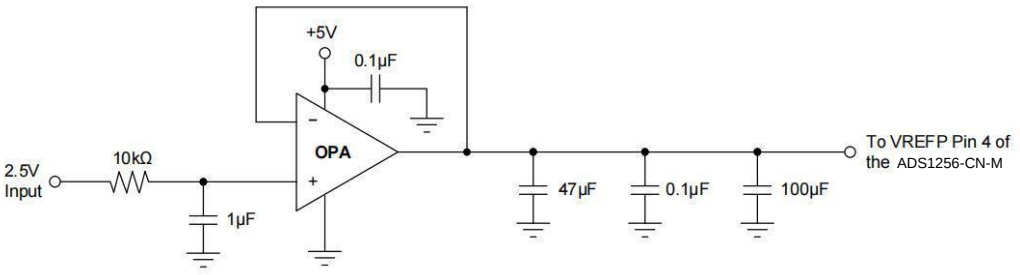


Figure 53 Recommended Reference Voltage Buffer Circuit

13. PACKAGE IMFORMATION

The ADS1255-CN-M is available in an SSOP-20 package;
The ADS1256-CN-M is available in an SSOP-28 package;

13.1 SSOP-20(ADS1255-CN-M)

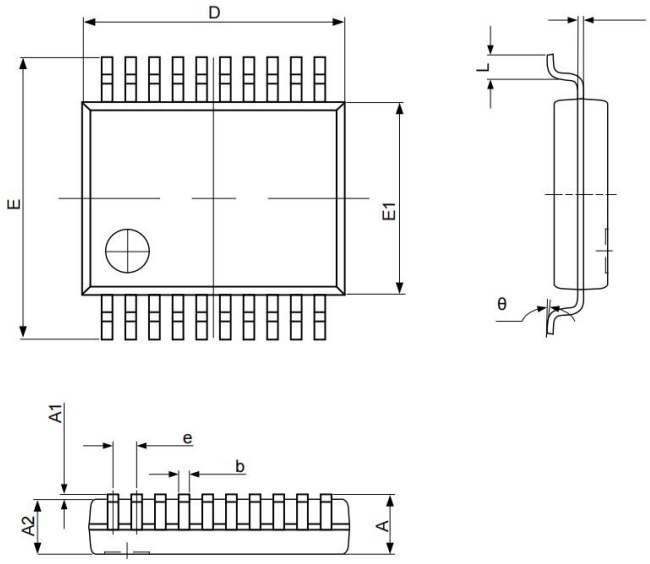


Figure 54 SSOP-20 Package Dimension Drawing

Table 53 SSOP-20 Package Dimension Table

SYMBOL	Dimensions (mm)		Dimensions (inch)	
	MIN	MAX	MIN	MAX
A	---	1.730	---	0.068
A1	0.050	0.230	0.002	0.009
A2	1.400	1.600	0.055	0.063
b	0.220	0.380	0.009	0.015
c	0.090	0.250	0.004	0.010
D	7.000	7.400	0.276	0.291
E	7.600	8.000	0.299	0.315
E1	5.100	5.500	0.201	0.217
e	0.65 (BSC)		0.026 (BSC)	
L	0.550	0.950	0.022	0.037
θ	0°	8°	0°	8°

13.2 SSOP-28(ADS1256-CN-M)

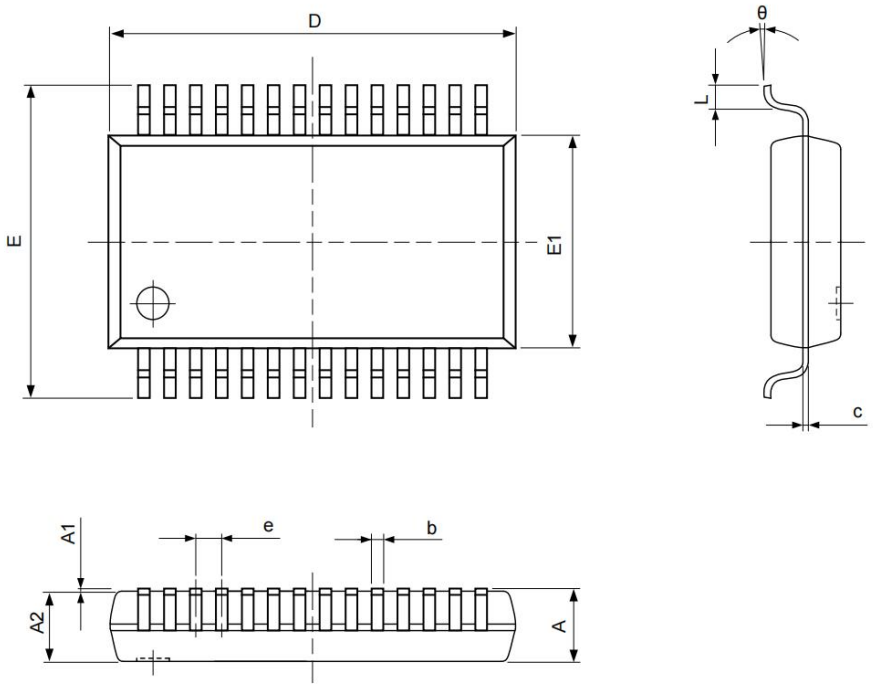


Figure 55 SSOP-28 Package Dimension Drawing

Table 54 SSOP-28 Package Dimension Table

SYMBOL	Dimensions（mm）		Dimensions（inch）	
	MIN	MAX	MIN	MAX
A	---	2.000	---	0.079
A1	0.050	---	0.002	---
A2	1.650	1.850	0.065	0.073
b	0.220	0.380	0.009	0.015
c	0.090	0.250	0.004	0.010
D	9.900	10.500	0.390	0.413
E	7.400	8.200	0.291	0.323
E1	5.000	5.600	0.197	0.220
e	0.650 (BSC)		0.026 (BSC)	
L	0.550	0.950	0.022	0.037
θ	0°	8°	0°	8°

NOTICE

The information presented in this document is for reference only. Involving product optimization and productivity improvement, ChipNobo reserves the right to adjust product indicators and upgrade some technical parameters. ChipNobo is entitled to be exempted from liability for any delay or non-delivery of the information disclosure process that occurs.
本文件中提供的信息仅供参考。涉及产品优化和生产效率改善，ChipNobo 有权调整产品指标和部分技术参数的升级，所出现信息披露过程存在延后或者不能送达的情形，ChipNobo 有获免责权。

The product listed herein is designed to be used with residential and commercial equipment, and do not support sensitive items and specialized equipment in areas where sanctions do exist. ChipNobo Co., Ltd or anyone on its behalf, assumes no responsibility or liability for any damages resulting from improper use.
此处列出的产品旨在民用和商业设备上使用，不支持确有制裁地区的敏感项目和特殊设备，ChipNobo 有限公司或其代表，对因不当使用而造成的任何损害不承担任何责任。

For additional information, please visit our website https://www.chipnobo.com/en or consult your nearest Chipnobo sales office for further assistance.
欲了解更多信息，请访问我们的网站 https://www.chipnobo.com/en，或咨询离您最近的 Chipnobo 销售办事处以获得进一步帮助。