1. Features

- Band: 30MHz to 6000MHz
- Supports TDD and FDD operation
- Tunable channel bandwidth: <200 kHz to 60 MHz
- Dual receiver: 6 differential or 12 single-ended inputs
- Superior receiver sensitivity with a noise figure of 3dB
- RX gain maximum adjustment range:102dB (52dB analogue and 50dB digital)
- Real-time monitoring and control signals for manual gain
- Independent automatic gain control
- Dual transmitters: 4 differential outputs
- TX power maximum adjustment range: 98dB (48dB analogue and 50dB digital)
- TX EVM: ≤ -40dB
- TX noise: ≤-157dBm/Hz noise floor
- TX monitor: ≥42dB dynamic range with 1dB accuracy
- Integrated fractional-N synthesizer
- Multichip synchronization
- CMOS/LVDS digital interface

2. Applications

- General-purpose radio systems
- Femtocell/Picocell/Microcell base stations
- Multifunctional smart terminals
- Point-to-point communication systems

3. General description

The AD9361-CN is a high-performance, highly integrated ultra-wideband SDR transceiver that can be widely used in almost all modern digital wireless communication systems. The AD9361-CN receiver LO operates from 30MHz to 6GHz. Channel bandwidth from less than 200KHz to 56MHz are supported.

The AD9361-CN integrates a 12bits ADC and a 12bits DAC. The built-in programmable analog filter supports a minimum 0.7MHz bandwidth and a maximum 30MHz bandwidth for TX/RX analog low-pass filter. The mixer and phase-locked loop are also integrated inside the chip, and the transmit path includes a driver amplifier, making it possible to output more than 8dBm single tone.

The AD9361-CN uses a direct conversion architecture to achieve high modulation accuracy and ultra-low noise. The chip supports image suppression calibration, LO leakage calibration,transmit powermonitoring, spurious suppression, and receive channel gain calibration. Moreover, it has multi-chip synchronization function, which is suitable for multi-chip joint use scenario, such as MIMO. The AD9361-CN analogue RF power supply mainly uses 1 .3 V, while the digital part of the interface power supply uses 3.3 V or 2.5 V. The chip register read/write control uses the standard four-wire SPI. The AD9361-CN is packaged in a 10 mm x 10 mm, 144-ball chip scale package ball grid array (CSP_BGA).

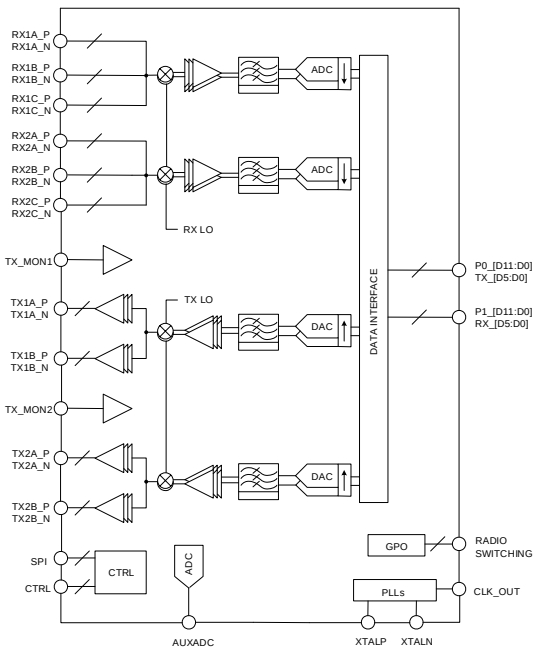


Figure 1 System diagram

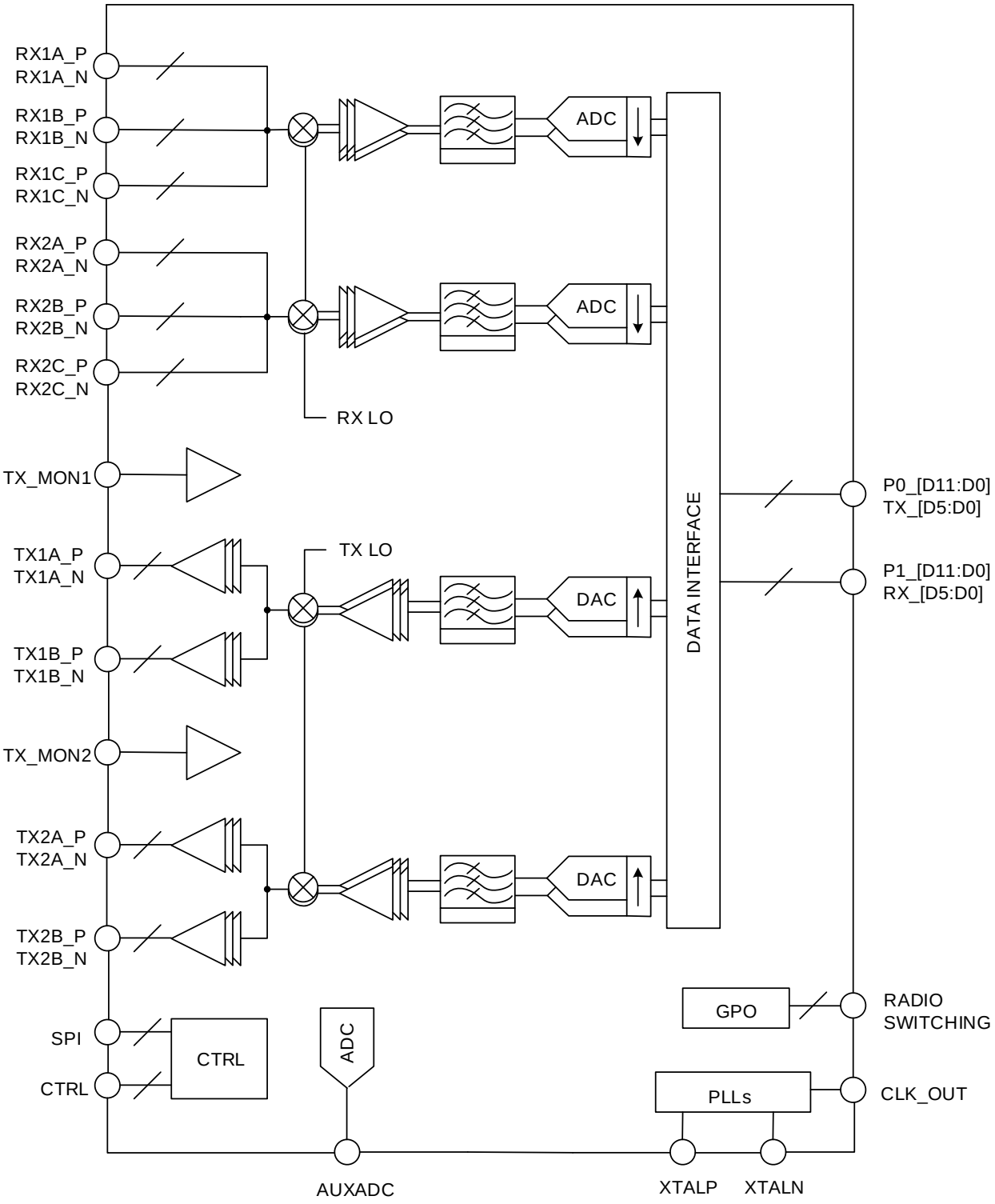


Figure 1 System diagram of AD9361-CN

6. Product specifications

6.1 Absolute maximum ratings

Parameter	Rating
VDDx to VSSx	-0.3V~ +1.4V
VDD_INTERFACE to VSSx	-0.3V~ +3.0V
VDD_GPO to VSSx	-0.3V~ +3.9V
Logical inputs and outputs to VSSx	-0.3V to VDD_INTERFACE+0.3V
Input current to any pin except power supply pins	±10mA
RF inputs (peak power)	2.5dBm
TX monitor input power (peak power)	9dBm
Maximum junction temperature (TJMAX)	110℃
Operating temperature range	-40~85℃
Storage temperature range	-55~125℃

Note: Exceeding the absolute maximum rating above may result in permanent damage to the device. This is the maximum rating only and cannot be used to infer the normal operation of the device under these conditions or any other conditions beyond the specifications indicated in the operating section of this Technical specification. Prolonged operation under absolute maximum rating conditions will affect the reliability of the device.

6.2 Recommended working conditions

Parameters	Recommended Values
VDDx	+1.3V
VDD_GPO	+1.8V~+3.3V
VDD_INTERFACE	+1.2V~+2.5V
Working ambient temperature	-45~85℃

6.3 Thermal characteristics

Parameter	Value
Thermal resistance	27.2℃/W

6.4 Reflux temperature curve

The AD9361-CN reflux temperature curve is based on the JEDEC JESD20 device standard. The maximum reflux temperature is +260℃.

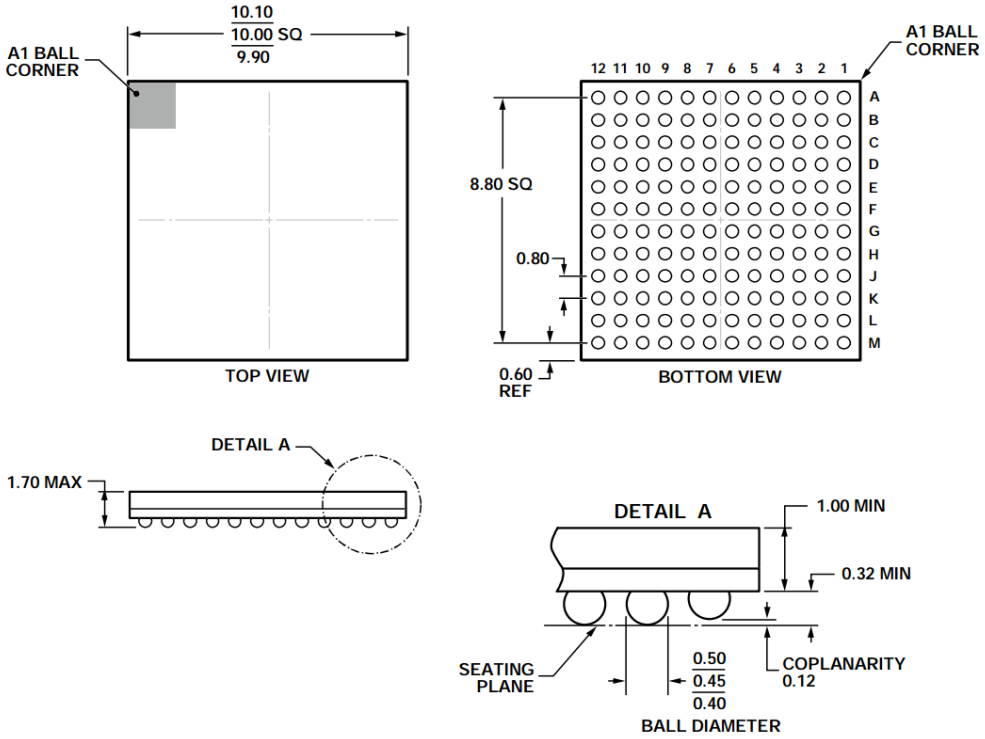
6.5 ESD caution

ESD (electrostatic discharge) sensitive devices

Live devices and circuit boards may be powered down without being noticed. Although this product has a patented or proprietary protection circuit, the device may be damaged when exposed to high energy ESD. Therefore, appropriate ESD protection measures should be taken to avoid degradation of device performance or loss of function.

7. Package and pin function descriptions

7.1 Outline dimensions (in millimeters)



7.2 Pin function descriptions

	1	2	3	4	5	6	7	8	9	10	11	12
A	RX2A_N	RX2A_P	NC	VSSA	TX_MON2	VSSA	TX2A_P	TX2A_N	TX2B_P	TX2B_N	NC	TX_EXT_LO_IN
B	VSSA	VSSA	NC	GP0_3	GP0_2	GP0_1	GP0_0	VDD_GPO	VDD1P3_RF	NC	NC	VSSA
C	RX2B_P	VSSA	NC	TEST/ ENABLE	CTRL_IN0	CTRL_IN1	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
D	RX2B_N	VDD1P3_ TX2	AVDD13_ ADDA2	CTRL_OUT0	CTRL_IN3	CTRL_IN2	P0_D9/ TX_D4_P	P0_D7/ TX_D3_P	P0_D5/ TX_D2_P	P0_D3/ TX_D1_P	P0_D1/ TX_D0_P	VSSD
E	RX2C_P	VDD1P3_RX	NC	CTRL_OUT1	CTRL_OUT2	CTRL_OUT3	P0_D11/ TX_D5_P	P0_D8/ TX_D4_N	P0_D6/ TX_D3_N	P0_D4/ TX_D2_N	P0_D2/ TX_D1_N	P0_D0/ TX_D0_N
F	RX2C_N	VDD1P3_RX	VSSA	CTRL_OUT6	CTRL_OUT5	CTRL_OUT4	VSSD	P0_D10/ TX_D5_N	VSSD	FB_CLK_P	VSSD	VDDD1P3_ DIG
G	RX_EXT_ LO_IN	NC	NC	CTRL_OUT7	EN_AGC	ENABLE	RX_ FRAME_N	RX_ FRAME_P	TX_ FRAME_P	FB_CLK_N	DATA_ CLK_P	VSSD
H	RX1C_N	VSSA	VSSA	TXNRX	SYNC_IN	VSSA	VSSD	P1_D11/ RX_D5_P	TX_ FRAME_N	VSSD	DATA_ CLK_N	VDD_ INTERFACE
J	RX1C_P	VSSA	AVDD13_ ADDA1	SPI_DI	SPI_CLK	CLK_OUT	P1_D10/ RX_D5_N	P1_D9/ RX_D4_P	P1_D7/ RX_D3_P	P1_D5/ RX_D2_P	P1_D3/ RX_D1_P	P1_D1/ RX_D0_P
K	RX1B_N	VSSA	VDD1P3_ TX1	AVDD13 _LFCK	RESETB	SPI_ENB	P1_D8/ RX_D4_N	P1_D6/ RX_D3_N	P1_D4/ RX_D2_N	P1_D2/ RX_D1_N	P1_D0/ RX_D0_N	VSSD
L	RX1B_P	VSSA	VSSA	RBIAS	NC	SPI_DO	VSSA	VSSA	VSSA	VSSA	VSSA	VSSA
M	RX1A_N	RX1A_P	NC	VSSA	TX_MON1	VSSA	TX1A_P	TX1A_N	TX1B_P	TX1B_N	XTALP	XTALN

Pin Number	Type	Pin name	Description
A1,A2	I	RX2A_N,RX2A_P	Receive channel 2 Differential input A. Alternatively, each pin can be used as a single-ended input. Tie unused pins to ground with a capacitor
A3, A11,B3,B10,B11, C3,E3,G2,G3, L5,M3	NC	NC	No Connect
A4,A6,B1,B2,B12,C2, C7 to C12,F3,H2,H3, H6,J2,K2,L2,L3, L7 to L12,M4,M6	I	VSSA	Analog ground
A5	I	TX_MON2	Transmit channel 2 power monitoring input. Tie to ground with a capacitor when not used
A7,A8	O	TX2A_P, TX2A_N	Transmit channel 2 Differential output A. If unused, do not connect these pins
A9,A10	O	TX2B_P,TX2B_N	Transmit channel 2 differential output B. If unused, do not connect these pins
A12	I	TX_EXT_LO_IN	External LO input. If unused, tie to ground
B4 to B7	O	GPO_3 to GPO_0	3.3V general-purpose outputs
B8	I	VDD_GPO	GPO 2.5V to 3.3V supply. Connect to 1.3V if unused
B9	I	VDD1P3_RF	RF 1.3V power supply input
C1,D1	I	RX2B_P,RX2B_N	Receive channel 2 Differential input B. Alternatively, each pin can be used as a single-ended input. Tie unused pins to ground with a capacitor
C4	I	TEST/ENABLE	Test input. In normal operation, tie this pin to ground
C5,C6,D5,D6	I	CTRL_IN0 to CTRL_IN3	Control input. Manual RX gain and TX attenuation control
D2	I	VDD1P3_TX2	TX2 1.3V power supply input, connect to D3
D3	I	AVDD13_ADDA2	ADC2/DAC2 1.3V power supply input
D4,E4 to E6,F4 to F6,G4	O	CTRL_OUT0,CTRL_OUT1 to CTRL_OUT3,CTRL_OUT6 to CTRL_OUT4,CTRL_OUT7	Control Outputs. These pins are multipurpose outputs that have programmable functionality
D7	I/O	P0_D9/TX_D4_P	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D9, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D4_P) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
D8	I/O	P0_D7/TX_D3_P	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D7, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D3_P) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
D9	I/O	P0_D5/TX_D2_P	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D5, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D2_P) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
D10	I/O	P0_D3/TX_D1_P	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D3, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D1_P) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.

Pin Number	Type	Pin name	Description
D11	I/O	P0_D1/TX_D0_P	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D1, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D0_P) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
D12, F7, F9,F11, G12, H7,H10, K12	I	VSSD	Digital ground
E1, F1	I	RX2C_P, RX2C_N	Receive channel 2 Differential input C. Alternatively, each pin can be used as a single-ended input. Tie unused pins to ground with a capacitor
E2	I	VDD1P3_RX	Receive 1.3V power supply input
E7	I/O	P0_D11/TX_D5_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D11, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D5_P) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
E8	I/O	P0_D8/TX_D4_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D8, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D4_N) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
E9	I/O	P0_D6/TX_D3_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D6, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D3_N) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
E10	I/O	P0_D4/TX_D2_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D4, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D2_N) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
E11	I/O	P0_D2/TX_D1_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D2, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D1_N) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
E12	I/O	P0_D0/TX_D0_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D0, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D0_N) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
F2	I	VDDA1P3_RX_VCO_LDO	Receive VCO LDO 1.3V power supply input
F8	I/O	P0_D10/TX_D5_N	Digital Data Port P0/Transmit Differential Input Bus. This is a dual function pin. As P0_D10, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 0. Alternatively, this pin (TX_D5_N) can function as part of the LVDS 6-bit TX differential input bus with internal LVDS termination.
F10, G10	I	FB_CLK_P, FB_CLK_N	Feedback Clock. These pins receive the FB_CLK signal that clocks in TX data. In CMOS mode, use FB_CLK_P as the input and tie FB_CLK_N to ground
F12	I	VDDD1P3_DIG	1.3V digital power supply input
G1	I	RX_EXT_LO_IN	External Receive LO Input. If this pin is unused, tie it to ground
G5	I	EN_AGC	Manual control input for automatic gain control (AGC)
G6	I	ENABLE	Control input. This pin moves the device through various operational states

Pin Number	Type	Pin name	Description
G7,G8	O	RX_FRAME_N, RX_FRAME_P	Receive Digital Data Framing Output Signal. These pins transmit the RX_FRAME signal that indicates whether the RX output data is valid. In CMOS mode, use RX_FRAME_P as the output and leave RX_FRAME_N unconnected.
G9, H9	I	TX_FRAME_P, TX_FRAME_N	Transmit Digital Data Framing Input Signal. These pins receive the TX_FRAME signal that indicates when TX data is valid. In CMOS mode, use TX_FRAME_P as the input and tie TX_FRAME_N to ground.
G11, H11	O	DATA_CLK_P, DATA_CLK_N	Receive Data Clock Output. These pins transmit the DATA_CLK signal that is used by the BBP to clock RX data. In CMOS mode, use DATA_CLK_P as the output and leave DATA_CLK_N unconnected.
H1, J1	I	RX1C_N, RX1C_P	Receive channel 1 Differential input C. Alternatively, each pin can be used as a single-ended input. Tie unused pins to ground with a capacitor
H4	I	TXNRX	Enable state machine control signals. This pin controls the data port bus direction. Logic low selects the RX direction and logic high selects the TX direction
H5	I	SYNC_IN	Used to synchronize digital clocks between multiple AD9361-CN devices. If this pin is unused, tied it to ground
H8	I/O	P1_D11/RX_D5_P	Digital Data Port P1/Transmit Differential Input Bus. This is a dual function pin. As P1_D11, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D5_P) can function as part of the LVDS 6-bit RX differential input bus with internal LVDS termination.
H12	I	VDD_INTERFACE	1.2V to 2.5V Supply for Digital I/O Pins (1.8V to 2.5V in LVDS Mode).
J3	I	AVDD13_ADDA1	ADC1/DAC1 1.3V power supply input
J4	I	SPI_DI	SPI serial data input
J5	I	SPI_CLK	SPI clock input
J6	O	CLK_OUT	Output Clock. This pin can be configured to output either a buffered version of the external input clock, the DCXO, or a divided-down version of the internal ADC_CLK
J7	I/O	P1_D10/RX_D5_N	Digital Data Port P1/Transmit Differential Input Bus. This is a dual function pin. As P1_D10, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D5_N) can function as part of the LVDS 6-bit RX differential input bus with internal LVDS termination.
J8	I/O	P1_D9/RX_D4_P	Digital Data Port P1/Transmit Differential Input Bus. This is a dual function pin. As P1_D9, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D4_P) can function as part of the LVDS 6-bit RX differential input bus with internal LVDS termination.
J9	I/O	P1_D7/RX_D3_P	Digital Data Port P1/Transmit Differential Input Bus. This is a dual function pin. As P1_D7, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D3_P) can function as part of the LVDS 6-bit RX differential input bus with internal LVDS termination.
J10	I/O	P1_D5/RX_D2_P	Digital Data Port P1/Transmit Differential Input Bus. This is a dual function pin. As P1_D5, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D2_P) can function as part of the LVDS 6-bit RX differential input bus with internal LVDS termination.

Pin Number	Type	Pin name	Description
J11	I/O	P1_D3/RX_D1_P	Digital Data Port P1/Transmit Differential Input Bus. This is a dual function pin. As P1_D3, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively,this pin (RX_D1_P) can function as part of the LVDS 6-bit RX differential input bus with internal LVDS termination.
J12	I/O	P1_D1/RX_D0_P	Digital Data Port P1/Transmit Differential Input Bus. This is a dual function pin. As P1_D1, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D0_P) can function as part of the LVDS 6-bit RX differential input bus with internal LVDS termination.
K1, L1	I	RX1B_N, RX1B_P	Receive channel 1 Differential input B. Alternatively, each pin can be used as a single-ended input. Tie unused pins to ground with a capacitor
K3	I	VDD1P3_TX1	TX1 1.3V power supply input
K4	I	AVDD13_LFCK	SYSPLL/XO 1.3V power supply input
K5	I	RESETB	Asynchronous reset. Logic low resets the device
K6	I	SPI_ENB	SPI Enable input. Set this pin to logic low to enable the SPI bus
K7	I/O	P1_D8/RX_D4_N	Digital Data Port P1/Transmit Differential Input Bus. This is a dual function pin. As P1_D8, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D4_N) can function as part of the LVDS 6-bit RX differential input bus with internal LVDS termination.
K8	I/O	P1_D6/RX_D3_N	Digital Data Port P1/Transmit Differential Input Bus. This is a dual function pin. As P1_D6, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D3_N) can function as part of the LVDS 6-bit RX differential input bus with internal LVDS termination.
K9	I/O	P1_D4/RX_D2_N	Digital Data Port P1/Transmit Differential Input Bus. This is a dual function pin. As P1_D4, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D2_N) can function as part of the LVDS 6-bit RX differential input bus with internal LVDS termination.
K10	I/O	P1_D2/RX_D1_N	Digital Data Port P1/Transmit Differential Input Bus. This is a dual function pin. As P1_D21, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D1_N) can function as part of the LVDS 6-bit RX differential input bus with internal LVDS termination.
K11	I/O	P1_D0/RX_D0_N	Digital Data Port P1/Transmit Differential Input Bus. This is a dual function pin. As P1_D0, it functions as part of the 12-bit bidirectional parallel CMOS level Data Port 1. Alternatively, this pin (RX_D0_N) can function as part of the LVDS 6-bit RX differential input bus with internal LVDS termination.
L4	I	RBIAS	Bias Input Reference. Connect this pin through a 14.3 kΩ (1% tolerance) resistor to ground
L6	O	SPI_DO	SPI Serial Data Output in 4-Wire Mode,or High-Z in 2-Wire Mode.
M1,M2	I	RX1A_N, RX1A_P	Receive channel 1 Differential input A. Alternatively, each pin can be used as a single-ended input. Tie unused pins to ground with a capacitor
M5	I	TX_MON1	Transmit channel 1 power monitoring input. Tie to ground with a capacitor if not used
M7,M8	O	TX1A_P, TX1A_N	Transmit channel 1 Differential output A. If unused, do not connect these pins
M9,M10	O	TX1B_P, TX1B_N	Transmit channel 1 Differential output B. If unused, do not connect these pins
M11,M12	I	XTALP, XTALN	Reference Frequency Crystal Connections. When a crystal is used, connect it between these two pins. When an external clock source is used, connect it to XTALN and leave XTALP unconnected

8. Specifications

8.1 Receiver

Electrical characteristics at VDD_GPO = 3.3V, VDD_INTERFACE = 2.5V, and all other VDDx pins = 1.3V, T_A= 25°C, unless otherwise noted.

Parameter	Min	Typ	Max	Unit	Test conditions/Comments
Center frequency	30		6000	MHz	
Channel bandwidth	0.2		60	MHz	
Min analog gain		10		dB	
Max analog gain	50	52	54	dB	52dB@2.4GHz
Analog gain step		1		dB	
Min digital gain		0		dB	
Max digital gain		50		dB	
Digital gain step		0.25		dB	
Receiver 800MHz					
Noise figure		3		dB	Maximum RX gain
Third-Order Input Intermodulation Intercept Point		-13		dBm	Maximum RX gain
Second order Input Intermodulation Intercept Point		45		dBm	Maximum RX gain
Local oscillator (LO) leakage		-90		dBm	At RX front-end input
Modulation accuracy (EVM)		-40		dB	30.72MHz reference clock; LTE20M, QPSK
Input S11		-10		dB	
RX1 to RX2 isolation		50		dB	RX1A to RX2A,RX1B to RX2B
RX2 to RX1 isolation		50		dB	RX2A to RX1A,RX2B to RX1B
Receiver 2400MHz					
Noise figure		4		dB	Maximum RX gain
Third-Order Input Intermodulation Intercept Point		-13		dBm	Maximum RX gain
Second order Input Intermodulation Intercept Point		45		dBm	Maximum RX gain
Local oscillator (LO) leakage		-80		dBm	At RX front-end input
Modulation accuracy (EVM)		-40		dB	30.72MHz reference clock; LTE20M, QPSK
Input S11		-10		dB	
RX1 to RX2 isolation		50		dB	RX1A to RX2A,RX1B to RX2B
RX2 to RX1 isolation		50		dB	RX2A to RX1A,RX2B to RX1B

Parameter	Min	Typ	Max	Unit	Test conditions/Comments
Receiver 5500MHz					
Noise figure		6		dB	Maximum RX gain
Third-Order Input Intermodulation Intercept Point		-13		dBm	Maximum RX gain
Second order Input Intermodulation Intercept Point		45		dBm	Maximum RX gain
Local oscillator (LO) leakage		-70		dBm	At RX front-end input
Modulation accuracy (EVM)		-40		dB	30.72MHz reference clock; LTE20M, QPSK
Input S11		-10		dB	
RX1 to RX2 isolation		50		dB	RX1A to RX2A,RX1B to RX2B
RX2 to RX1 isolation		50		dB	RX2A to RX1A,RX2B to RX1B

8.2 Transmitter

Electrical characteristics at VDD_GPO = 3.3V, VDD_INTERFACE = 2.5V, and all other VDDx pins = 1.3V, T_A= 25°C, unless otherwise noted.

Parameter	Min	Typ	Max	Unit	Test conditions/Comments
Center frequency	30		6000	MHz	
Channel bandwidth	0.2		60	MHz	
Analog power control range	46	48	50	dB	48dB@2.4GHz
Analog power control step		1		dB	
Digital gain control range		50		dB	
Digital gain control step		0.125		dB	
TX Monitor (TX_MON1/TX_MON2)					
Maximum input level		4		dBm	
Dynamic range		42		dB	
Accuracy		1		dB	
Transmitter 800MHz					
Output S22		-10		dB	
Maximum output power		8		dBm	Single tone
Modulation accuracy (EVM)		-40		dB	30.72MHz reference clock; LTE20M, QPSK
Third order output Intermodulation Intercept Point		23		dBm	
Carrier leakage		-50		dBc	0 dB attenuation

Parameter	Min	Typ	Max	Unit	Test conditions/Comments
Carrier leakage		-32		dBc	40 dB attenuation
Image suppression		-55		dBc	
Noise floor		-157		dBm/Hz	
TX1 to TX2 Isolation		50		dB	
TX2 to TX1 Isolation		50		dB	
Transmitter 2400MHz					
Output S22		-10		dB	
Maximum output power		7.5		dBm	Single tone
Modulation accuracy (EVM)		-40		dB	30.72MHz reference clock; LTE20M, QPSK
Third order output Intermodulation Intercept Point		19		dBm	
Carrier leakage		-50		dBc	0 dB attenuation
Carrier leakage		-32		dBc	40 dB attenuation
Image suppression		-55		dBc	
Noise floor		-156		dBm/Hz	
TX1 to TX2 Isolation		50		dB	
TX2 to TX1 Isolation		50		dB	
Transmitter 5500MHz					
Output S22		-10		dB	
Maximum output power		6		dBm	Single tone
Modulation accuracy (EVM)		-36		dB	30.72MHz reference clock; LTE20M, QPSK
Third order output Intermodulation Intercept Point		17		dBm	
Carrier leakage		-50		dBc	0 dB attenuation
Carrier leakage		-30		dBc	40 dB attenuation
Image suppression		-55		dBc	
Noise floor		-151		dBm/Hz	
TX1 to TX2 Isolation		50		dB	
TX2 to TX1 Isolation		50		dB	

8.3 LO Synthesizer specifications

Electrical characteristics at VDD_GPO = 3.3V, VDD_INTERFACE = 2.5V, and all other VDDx pins = 1.3V, T_A= 25°C, unless otherwise noted.

Parameter	Min	Typ	Max	Unit	Test conditions/Comments
Reference clock					
Reference clock (crystal input)	19		50	MHz	
Reference clock(external oscillator)	10		80	MHz	
Local oscillator frequency synthesizer					
Local oscillator resolution		2.4		Hz	
Integral phase noise (10KHz~100MHz)		0.13		°rms	800MHz
		0.32		°rms	2400MHz
		0.60		°rms	5500MHz
Baseband frequency synthesizer					
Output frequency range	2000		3800	MHz	

8.4 Power consumption

Electrical characteristics at VDD_GPO = 3.3V, VDD_INTERFACE = 2.5V, and all other VDDx pins = 1.3V, T_A= 25°C, unless otherwise noted.

Parameter	Min	Typ	Max	Unit	Test conditions/Comments
1TX power consumption		320		mW	7dBm output at 20M bandwidth in 2.4G band
1RX power consumption		230		mW	Maximum RX gain at 20M bandwidth in 2.4G band

9. Theory of operation

9.1 General characteristics

The AD9361-CN is highly integrated radio frequency (RF) transceiver capable of being configured for a wide range of applications. The device integrates all RF, mixed signal, and digital blocks necessary to provide all transceiver functions in a single device. Programmability allows this broadband transceiver to be adapted for use with multiple communication standards, including frequency division duplex (FDD) and time division duplex (TDD) systems. This programmability also allows the device to be interfaced to various baseband processors (BBPs) using a single 12-bit parallel data port, dual 12-bit parallel data ports, or a 12-bit low voltage differential signaling (LVDS) interface.

The AD9361-CN also provides self-calibration and automatic gain control (AGC) systems to maintain a high performance level under varying temperatures and input signal conditions.

9.2 Receiver

The receiver section contains all blocks necessary to receive RF signals and convert them to digital data that is usable by a BBP. There are two independently controlled channels that can receive signals from different sources, allowing the device to be used in multiple input, multiple output (MIMO) systems while sharing a common frequency synthesizer. Each channel has three inputs that can be multiplexed to the signal chain, making the AD9361-CN suitable for use in diversity systems with multiple antenna inputs. The receiver is a direct conversion system that contains a mixer and band shaping filter that down convert received signals to baseband for digitization. Gain control is achieved by following a preprogrammed gain index map that distributes gain among the blocks for optimal performance at each level. This can be achieved by enabling the internal AGC in either fast or slow mode or by using manual gain control, allowing the BBP to make the gain adjustments as needed. Additionally, each channel contains independent RSSI measurement capability, dc offset tracking, and all circuitry necessary for self-calibration. The receiver includes 12-bit SAR ADCs and adjustable sample rates that produce data streams from the received signals. The digitized signals can be conditioned further by a series of decimation filters and a fully programmable 128-tap FIR filter with additional decimation settings. The sample rate of each digital filter block is adjustable by changing decimation factors to produce the desired output data rate.

9.3 Transmitter

The transmitter section consists of two identical and independently controlled channels that provide all digital processing, mixed signal, and RF blocks necessary to implement a direct conversion system while sharing a common frequency synthesizer. The digital data received from the BBP passes through a fully programmable 128-tap FIR filter without interpolation options. The FIR output is sent to a series of interpolation filters that provide additional filtering and data rate interpolation prior to reaching the DAC. Each 12-bit DAC has an adjustable sampling rate. Both the I and Q channels are fed to the RF block for up conversion.

Self-calibration circuitry is built into each transmit channel to provide automatic real-time adjustment. The transmitter block also provides a TX monitor block for each channel. This block monitors the transmitter output and routes it back through an unused receiver channel to the BBP for signal monitoring. The TX monitor blocks are available only in TDD mode operation while the receiver is idle.

9.4 Clock input option

The AD9361-CN operates using a reference clock that can be provided by two different sources. The first option is to use a dedicated crystal with a frequency between 19MHz and 50MHz connected between the XTALP and XTALN pins. The second option is to connect an external oscillator or clock distribution device to the XTALN pin (with the XTALP pin remaining unconnected). If an external oscillator is used, the frequency can vary between 10MHz and 80MHz.

9.5 Frequency Synthesizers

RF PLLs

The AD9361-CN contains two identical synthesizers to generate the required LO signals for the RF signal paths: one for the receiver and one for the transmitter, and the transmitter TXLO can be shared to receivers if needed. Phase-locked loop (PLL) synthesizers are fractional-N designs incorporating completely integrated voltage controlled oscillators (VCOs) and loop filters. In TDD operation, the synthesizers turn on and off as appropriate for the RX and TX frames. In FDD mode, the TX PLL and the RX PLL can be activated simultaneously. These PLLs require no external components.

BB PLL

The AD9361-CN also contains a baseband PLL synthesizer that is used to generate all baseband related clock signals. These include the ADC and DAC sampling clocks, the DATA_CLK signal. This PLL is programmed from 2200 MHz to 300 MHz based on the data rate and sample rate requirements of the system.

9.6 Digital Data Interface

The AD9361-CN data interface uses parallel data ports (P0 and P1) to transfer data between the device and the BBP. The data ports can be configured in either single-ended CMOS format or differential LVDS format. Both formats can be configured in multiple arrangements to match system requirements for data ordering and data port connections. These arrangements include single port data bus, dual port data bus, single data rate, double data rate, and various combinations of data ordering to transmit data from different channels across the bus at appropriate times. Bus transfers are controlled using simple hardware handshake signaling. The two ports can be operated in either bidirectional (TDD) mode or in full duplex (FDD) mode where half the bits are used for transmitting data and half are used for receiving data.

The interface can also be configured to use only one of the data ports for applications that do not require high data rates and prefer to use fewer interface pins.

DATA_CLK signal

RX data supplies the DATA_CLK signal that the BBP can use when receiving the data. The DATA_CLK can be set to a rate that provides single data rate (SDR) timing where data is sampled on each rising clock edge, or it can be set to provide double data rate (DDR) timing where data is captured on both rising and falling edges. This timing applies to operation using either a single port or both ports.

FB_CLK signal

For transmit data, the interface uses the FB_CLK signal as the timing reference. FB_CLK allows source synchronous timing with rising edge capture for burst control signals and either rising edge (SDR mode) or both edge capture (DDR mode) for transmit signal bursts. The FB_CLK signal must have the same frequency and duty cycle as DATA_CLK.

RX_FRAME signal

The device generates an RX_FRAME output signal whenever the receiver outputs valid data. This signal has two modes: level mode (RX_FRAME stays high as long as the data is valid) and pulse mode (RX_FRAME pulses with a 50% duty cycle). Similarly, the BBP must provide a TX_FRAME signal that indicates the beginning of a valid data transmission with a rising edge. Similar to the RX_FRAME, the TX_FRAME signal can remain high throughout the burst or it can be pulsed with a 50% duty cycle.

9.7 Enable state machine

The AD9361-CN transceiver includes an enable state machine (ENSM) that allows real-time control over the current state of the device. The device can be placed in several different states during normal operation, including

- Standby - Energy saving, frequency synthesizers disabled
- Sleep – wait with all clocks/ BB PLL disabled
- TX - The TX signal chain enabled
- RX -- The RX signal chain enabled
- FDD -- TX and RX signal chains enabled
- Alarm - Frequency synthesizers enabled

ENSM has two possible control methods: SPI control and pin control.

SPI control Mode

In SPI control mode, the ENSM is controlled asynchronously by writing SPI registers to advance the current state to the next state. SPI control is considered asynchronous to the DATA_CLK because the SPI_CLK can be derived from a different clock reference and can still function properly. The SPI control ENSM method is recommended when real-time control of the synthesizers is not necessary. SPI control can be used for realtime control as long as the BBIC has the ability to perform timed SPI writes accurately.

Pin control mode

In pin control mode, the enable function of the ENABLE pin and the TXNRX pin allow real-time control of the current state. The ENSM allows TDD or FDD operation depending on the configuration of the corresponding SPI register. The ENABLE and TXNRX pin control method is recommended if the BBIC has extra control outputs that can be controlled in real time, allowing a simple 2-wire interface to control the state of the device. To advance the current state of the ENSM to the next state, the enable function of the ENABLE pin can be driven by either a pulse (edge detected internally) or a level. When a pulse is used, it must have a minimum pulse width of one FB_CLK cycle. In level mode, the ENABLE and TXNRX pins are also edge detected by the AD9361-CN and must meet the same minimum pulse width requirement of one FB_ CLK cycle. In FDD mode, the ENABLE and TXNRX pins can be remapped to serve as real-time RX and TX data transfer control signals. In this mode, the ENABLE pin enables or disables the receive signal path, and the TXNRX pin enables or disables the transmit signal path. In this mode, the ENSM is removed from the system for control of all data flow by these pins.

9.8 SPI interface

The AD9361-CN uses a serial peripheral interface (SPI) to communicate with the BBP. This interface can only be configured as a 4-wire interface with dedicated receive and transmit ports, or it can be configured as a 3-wire interface with a bidirectional data communication port.This bus allows the BBP to set all device control parameters using a simple address data serial bus protocol. Write commands follow a 24-bit format. The first 6 bits are used to set the bus direction and number of bytes to transfer. The next 10 bits set the address where data is to be written. The final eight bits are the data to be transferred to the specified register address (MSB to LSB). The AD9361-CN also supports an LSB-first format that allows the commands to be written in LSB to MSB format. In this mode, the register addresses are incremented for multibyte writes. Read commands follow a similar format with the exception that the first 16 bits are transferred on the SPI_DI pin and the final eight bits are read from the AD9361-CN, which is done on the SPI_DO pin in 4-wire mode or on the SPI_DI pin in 3-wire mode.

9.9 General control pins

Control outputs (CTRL_OUT[7:0])

The AD9361-CN provides eight simultaneous real-time output signals for use as interrupts to the BBP. These outputs can be configured to output a number of internal settings and measurements that the BBP can use when monitoring transceiver performance in different situations. The control output pointer register selects what information is output to these pins, and the control output enable register determines which signals are activated for monitoring by the BBP. Signals used for manual gain mode, calibration flags, state machine states, and the ADC output are among the outputs that can be monitored on these pins.

Control inputs (CTRL_IN[3:0])

The AD9361-CN provides four edge detected control input pins. In manual gain mode, the BBP can use these pins to change the gain table index in real time. In transmit mode, the BBP can use two of the pins to change the transmit gain in real time.

GPO pins(GPO_3 至 GPO_0)

The AD9361-CN offers four 3.3 V capable general-purpose logic output pins: GPO_3, GPO_2, GPO_1, and GPO_0. These pins can be used to control other peripheral devices such as regulators and switches via the AD9361-CN SPI bus, or they can function as slaves for the internal AD9361-CN state machine.

9.10 Auxiliary converter AUXADC

The AD9361-CN contains an auxiliary ADC that can be used to monitor system functions such as temperature or power output. The converter is 12 bits wide and has an input range of 0 V to 1.25 V. When enabled, the ADC is in a free running state. SPI reads provide the last value latched at the ADC output. A multiplexer in front of the ADC allows the user to select between the AUXADC input pin and a built-in temperature sensor.

9.11 AD9361-CN power supply

The AD9361-CN must be powered by the following three supplies: the analog supply (VDDD1P3_DIG/VDDAx = 1.3 V), the interface supply (VDD_INTERFACE = 2.5V or 1.8V), and the GPO supply (VDD_GPO = 3.3 V). For applications requiring optimal noise performance, it is recommended that the 1.3 V supply be sourced from low noise, low dropout (LDO) regulators.

For applications that optimal noise performance is not critical but board space is important, the 1.3V power rail can be supplied directly from a switch and an integrated power management unit (PMU) can be adopted.

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