AD620SQ-CN/883B

High Performance, Low Power Instrumentation Amplifier

1. FEATURES

- **Easy to use**
  - **Gain set with one external resistor (Gain range 1 to 10,000)**
  - **Wide power supply range (±2 V to ±19 V)**
  - **Higher performance than 3 op amp IA designs**
  - **Available in 8-lead SOIC packaging**
  - **Low power, 1.57mA quiescent current**
- **Excellent dc performance**
  - **13 μV max, input offset voltage**
  - **3.1 nA max, input bias current**
  - **100 dB min common-mode rejection ratio (G = 10)**
- **Low noise**
  - **14nV/√Hz @ 1 kHz, input voltage noise**
  - **3 μV pp noise (0.1 Hz to 10 Hz)**
- **Excellent ac specifications**
  - **1300 kHz bandwidth (G = 1)**
  - **75 μs settling time to 0.01%**
- **Operating temperature:-55°C to 125°C**

2. APPLICATIONS

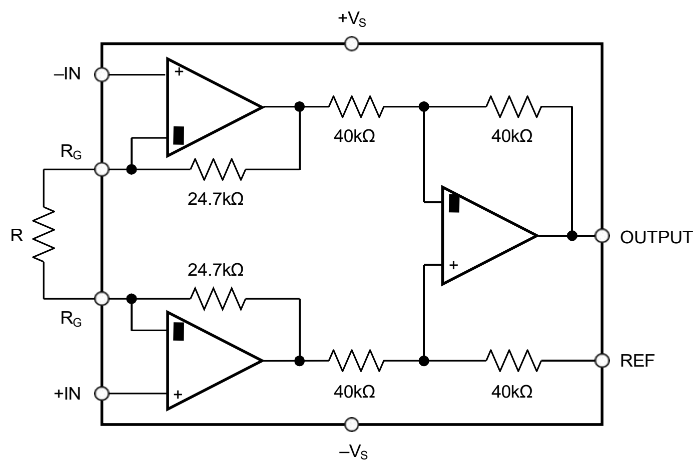
- **Weigh scales**
- **ECG and medical instrumentation**
- **Transducer interface**
- **Data acquisition systems**
- **Industrial process controls**
- **Battery-powered and portable equipment**

3. PRODUCT DESCRIPTION

The AD620SQ-CN/883B is a low cost high accuracy instrumentation amplifier that requires only one external resistor to set gains of 1 to 10,000. Furthermore, the AD620SQ-CN/883B features 8-lead SOIC packaging that offers low standby power consumption(only1.57 mA), making it a good fit for battery-powered, portable(or remote) applications.

The AD620SQ-CN/883B is a high accuracy instrumentation amplifier with a low nonlinearity of only 0.8ppm low offset voltage of 13 μV max, is ideal for use in precision data acquisition systems, such as weigh scales and transducer interfaces. Furthermore, the low noise, low input bias currentand low power of the AD620SQ-CN/883B make it well suited for medical applications , such as ECG and noninvasive blood pressure monitors.

The AD620SQ-CN/883B works well as a preamplifier due to its low input voltage noise of 14 nV/√Hz at 1 kHz, 3 μVpp in the 0.1 Hz to 10 Hz band, and 0.35 pA/√Hz input current noise. Also, the AD620SQ-CN/883B is well suited for multiplexed applications with its settling time of 75 μs to 0.01%, and its cost is low enough toenable designs with one in-amp per channel.



4. CONNECTION DIAGRAM

Figure 1 shows the pin configuration

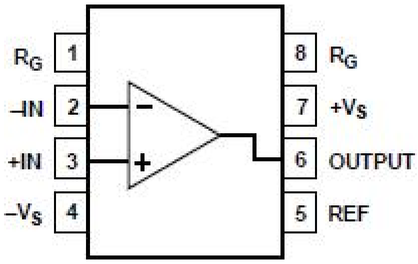


Figure 1. Pin Configuration

Table 1. Pin Function

Position	Name	Type	Description
1, 8	R_G	Analog output	Connect a resistor between two R_G to set gain. See more information in the **GAIN SELECTION** section.
2	–IN	Analog input	Signal negative input
3	+IN	Analog input	Signal positive input
4	$–V_S$	Power supply	Negative power supply
5	REF	Analog input	Output reference voltage input
6	OUTPUT	Analog output	Output
7	$+V_S$	Power supply	Positive power supply

5. PRODUCT SPECIFICATION

Table 2. Absolute Maximum Ratings

Parameter	Description	Min	Max	Units
Voltage	Supply		±20	V
	Input voltage	$-V_S - 0.3$	$+V_S + 0.3$	V
Internal Power Dissipation[(2)]			650	mW
Output Short-Circuit Duration		Indefinite		
Temperature	Operating, T_A	–55	125	°C
	Storage, $T_{stg,}$ Q	–65	150	
	Soldering, 10s		300	

Note 1: Stresses beyond those listed under **Table 3** may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under **Table 5**. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
Note 2: Specification is for device in free air—8-lead plastic package: θ_{JA} = 95°C.

Table 3. ESD Performance

Parameter	Symbol	Description	Value	Units
Electrostatic Discharge	$V_{(ESD)}$	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)], all pins except –IN and +IN	±2000	V
		Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)], –IN and +IN pin	±3500	
		Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)]	±2000	

Note 1: JEDEC document JEP155 states that 500V HBM allows safe manufacturing with a standard ESD control process.
Note 2: JEDEC document JEP157 states that 250V CDM allows safe manufacturing with a standard ESD control process.

Table 4. Recommended Working Conditions

Parameter	Description	Min	Nom	Max	Units
Operating Voltage Range	Split supply	±2	±18	±19	V
	Single supply	4	36	38	V
Specified Temperature Range		–55		125	°C

Table 5. Thermal Resistance Characteristics

Parameter	Symbol	SOIC-8	Units
Junction-to-Ambient Thermal Resistance	$R_{\theta JA}$	90.6	°C/W
Junction-to-Board Thermal Resistance	$R_{\theta JB}$	47.6	°C/W
Junction-to-Top Characterization Parameter	ψ_{JT}	3.6	°C/W
Junction-to-Board Characterization Parameter	ψ_{JB}	47	°C/W
Junction-to-Case (Top) Thermal Resistance	$R_{\theta JC(top)}$	35	°C/W
Junction-to-Case (Bottom) Thermal Resistance	$R_{\theta JC(bot)}$	50.8	°C/W

Table 6. Electrical Characteristics

Typical at 25°C,Vs=±18V,and R_L= 2kΩ to GND,unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
Gain					
Gain Range	G = 1 + (49.4kΩ / R_G)	1		10K	
Gain Error(1)	V_{OUT} = ±10V, G = 16		0.02	0.04	%
	V_{OUT} = ±10V, G = 10		0.03	0.08	%
	V_{OUT} = ±10V, G = 100		0.03	0.08	%
	V_{OUT} = ±10V, G = 1000		0.03	0.15	%
Nonlinearity	V_{OUT} = −10V to +10V, G = 1-10, R_L = 10kΩ		1		ppm
	V_{OUT} = −10V to +10V, G = 10-100, R_L = 10kΩ		10		ppm
	V_{OUT} = −10V to +10V, G = 100-1000, R_L = 10kΩ		50		ppm
Gain vs. Temperature	G = 1		1	2.5	ppm/°C
	Gain > 1(1)		3	26	ppm/°C
Voltage Offset(2)					
Input Offset, V_{OSI}	V_S = ±18V		±3.5	±13	μV
Output Offset, V_{OSO}	V_S = ±18V		±35	±240	μV
	V_S = ±2V to ±19V, overtemperature			±420	μV
	V_S = ±2V to ±19V, average TC		0.05		μV/°C
Offset Referred to The Input vs. Supply (PSR)	V_S = ±2V to ±20V, G = 1	108	133		dB
	V_S = ±2V to ±20V, G = 1, overtemperature	105			dB
	V_S = ±2V to ±20V, G = 10	125	140		dB
	V_S = ±2V to ±20V, G = 10, overtemperature	125			dB
	V_S = ±2V to ±20V, G = 100	130	144		dB
	V_S = ±2V to ±20V, G = 100, overtemperature	130			dB
	V_S = ±2V to ±20V, G = 1000	130	146		dB
	V_S = ±2V to ±20V, G = 1000, overtemperature	130			dB
Input Current					
Input Bias Current			1	3	nA
	Overtemperature			10	nA
Input Offset Current			0.6	2.2	nA
	Overtemperature			4.0	nA

Parameter	Conditions	Min	Typ	Max	Units
Input					
Input Impedance	Differential		34 || 5		GΩ_pF
	Common-Mode		34 || 6		GΩ_pF
Input Voltage Range(3)	V_S = ±2V to ±19V	$-V_S + 0.1$		$+V_S - 2$	V
Common-Mode Rejection					
Common-Mode Rejection Ratio DC to 60Hz With 1kΩ Source Imbalance	$V_{CM} = (-V_S + 0.1V)$ to $(+V_S - 2V)$, G = 1	97	114		dB
	$V_{CM} = (-V_S + 0.1V)$ to $(+V_S - 2V)$, G = 1, overtemp	90			dB
	$V_{CM} = (-V_S + 0.1V)$ to $(+V_S - 2V)$, G = 10	110	170		dB
	$V_{CM} = (-V_S + 0.1V)$ to $(+V_S - 2V)$, G = 10, overtemp	107			dB
	$V_{CM} = (-V_S + 0.1V)$ to $(+V_S - 2V)$, G = 100	129	159		dB
	$V_{CM} = (-V_S + 0.1V)$ to $(+V_S - 2V)$, G = 100, overtemp	128			dB
	$V_{CM} = (-V_S + 0.1V)$ to $(+V_S - 2V)$, G = 1000	145	182		dB
	$V_{CM} = (-V_S + 0.1V)$ to $(+V_S - 2V)$, G = 1000, overtemp	142			dB
Output					
Output Swing	R_L = 10kΩ, V_S = ±2V to ±19V, overtemperature	$-V_S + 0.2$		$+V_S - 0.3$	V
Short Circuit Current	Overtemperature		±23		mA
Dynamic Response					
Small Signal –3dB Bandwidth	G = 1		1300		kHz
	G = 10		230		kHz
	G = 100		28		kHz
	G = 1000		2.8		kHz
Slew Rate	G = 1, 10V step		1.6		V/μs
	G = 100, 10V step		0.5		V/μs
Settling Time to 0.01%, 10V Step	G = 1		75		μs
	G = 100		200		μs
Noise					
Voltage Noise, 1kHz(4)	Input, Voltage Noise, e_{ni}		14		nV/√Hz
	Output, Voltage Noise, e_{no}		70		nV/√Hz
RTI, 0.1Hz to 10Hz	G = 1		0.55		$μV_{PP}$
	G = 100		0.38		$μV_{PP}$
Current Noise	f = 1kHz		350		fA/√Hz
	0.1Hz to 10Hz		10		pA_{PP}

Parameter	Conditions	Min	Typ	Max	Units
Reference Input					
R_{IN}			40		kΩ
Voltage Range		$-V_S$		$+V_S$	V
Reference Gain to Output			1.2	27	μV/V
Power Supply					
Operating Range(5)		±2		±19	V
Quiescent Current	V_S = ±2V to ±19V		1.56	1.8	mA
Overtemperature				2	mA
Temperature Range					
For Specified Performance		−55		+125	°C

Note 1: Does not include effects of external resistor R_G.

Note 2: Total RTI Error = $V_{OSI} + V_{OSO} / G$

Note 3: One input grounded. G = 1.

Note 4: Total RTI Noise= $\sqrt{e^2ni + (e_{no} / G)^2}$

Note 5: This is defined as the same supply range that is used to specify PSR.

6. TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, V_S = ±15V, R_L = 2kΩ, unless otherwise noted.

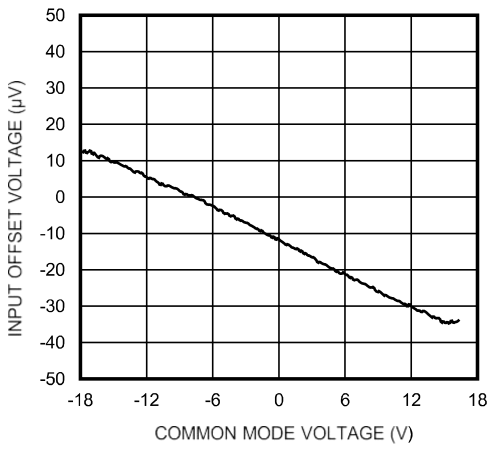


Figure 2. Input Offset Voltage vs. Common Mode Voltage

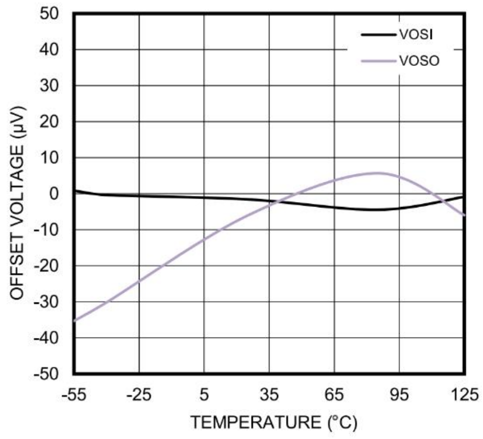


Figure 3. Input Offset Voltage vs. Temperature

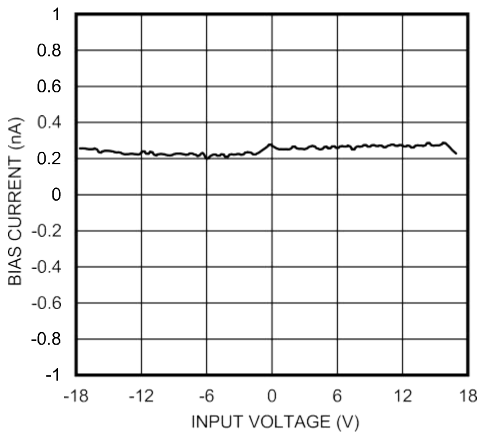


Figure 4. Input Bias Current vs. Common Mode Voltage (25°C)

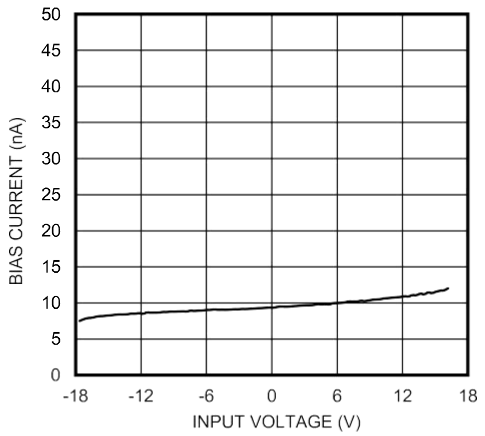


Figure 5. Input Bias Current vs. Common Mode Voltage (125°C)

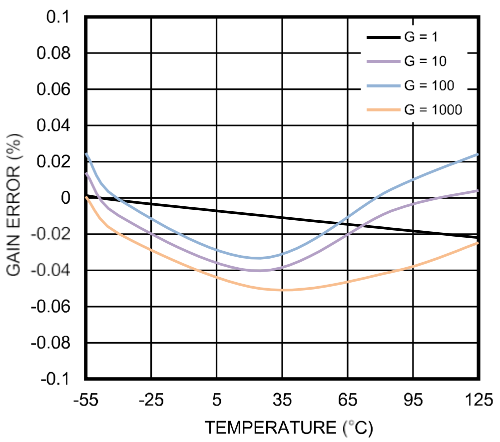


Figure 6. Gain vs. Temperature

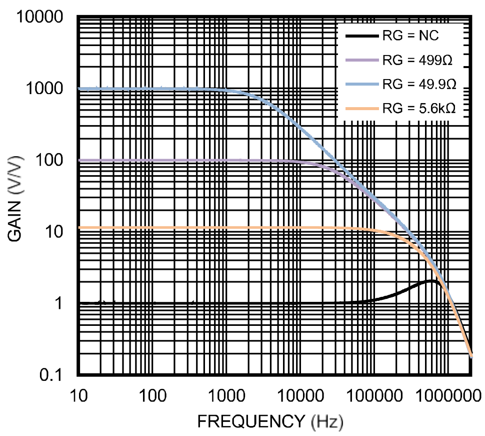


Figure 7. Gain vs. Frequency

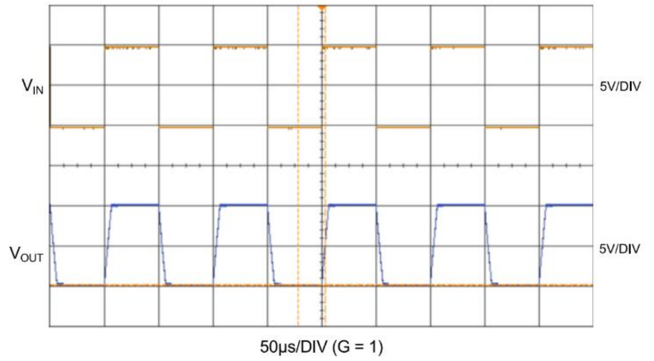


Figure 8. Large Signal Response (G = 1)

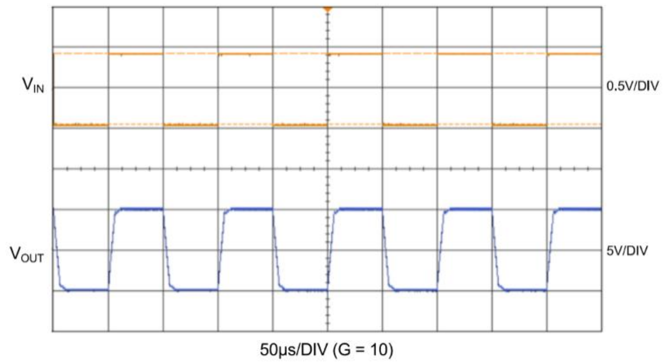


Figure 9. Large Signal Response (G = 10)

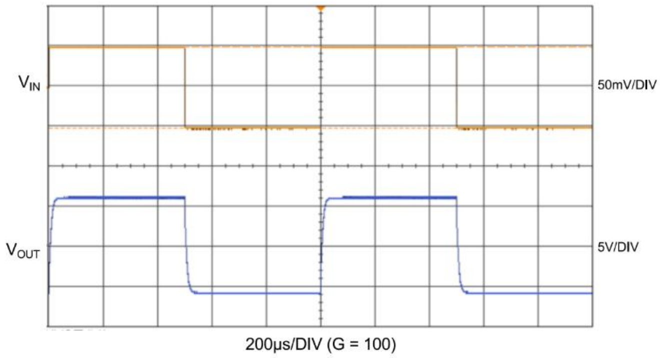


Figure 10. Large Signal Response (G = 100)

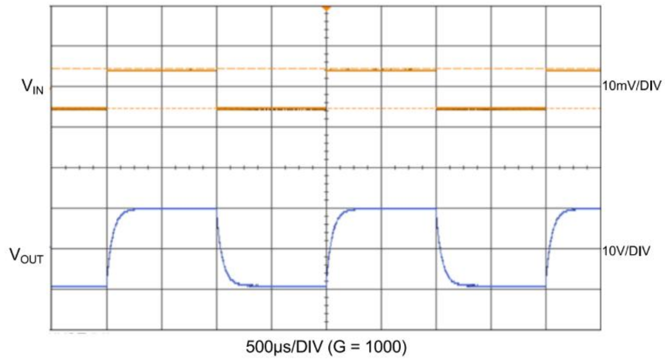


Figure 11. Large Signal Response (G = 1000)

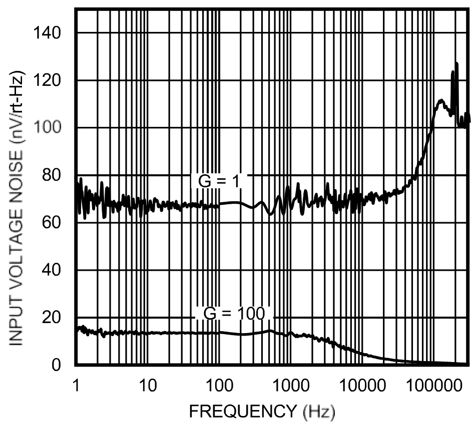


Figure 12. Input Offset Voltage Noise Density

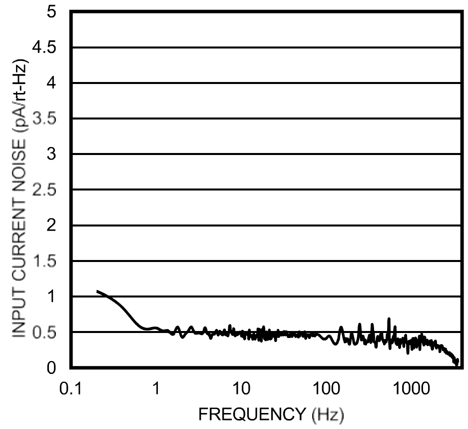


Figure 13. Input Bias Current Noise Density

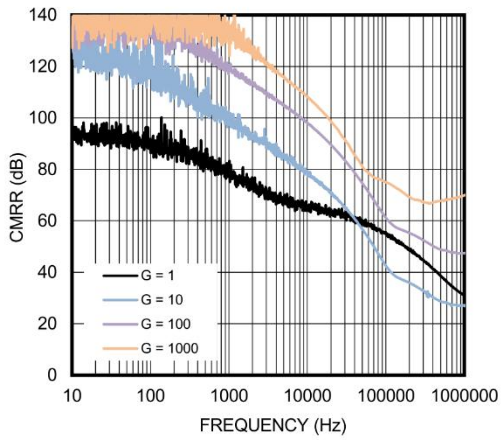


Figure 14. Positive PSR vs. Frequency

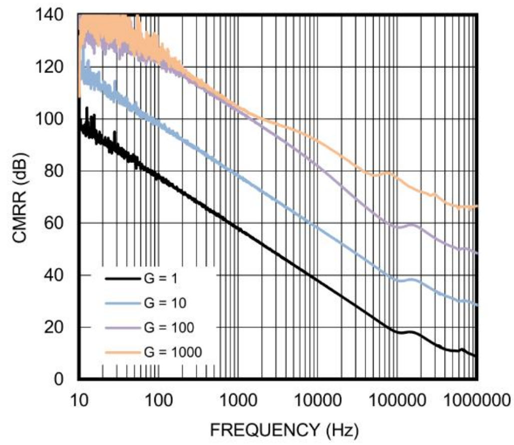


Figure 15. Negative PSR vs. Frequency

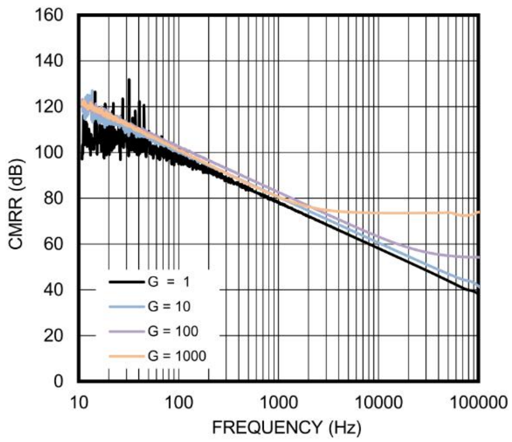


Figure 16. CMRR vs. Frequency

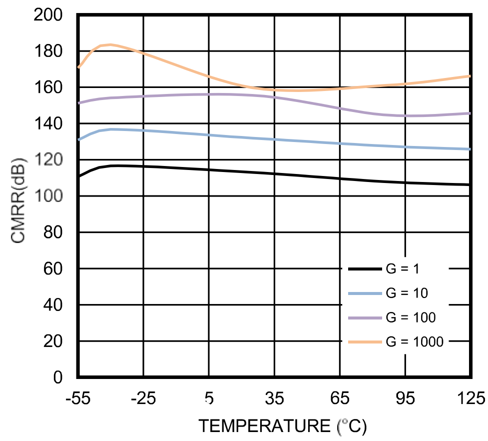


Figure 17. CMRR vs. Temperature

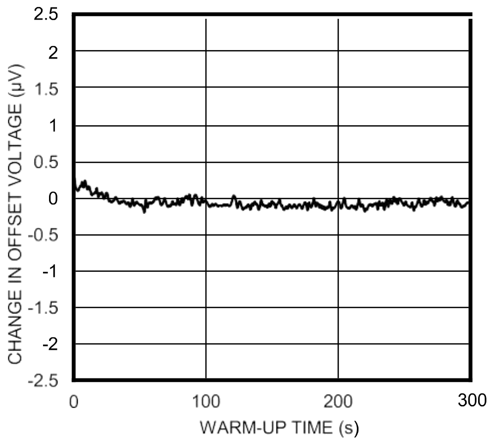


Figure 18. Warm-Up Time

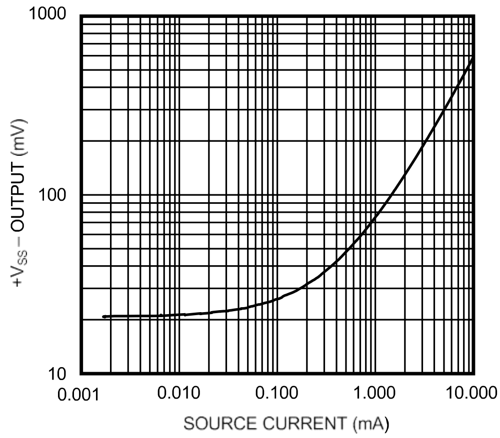


Figure 19. V_{OH} vs. Source Current

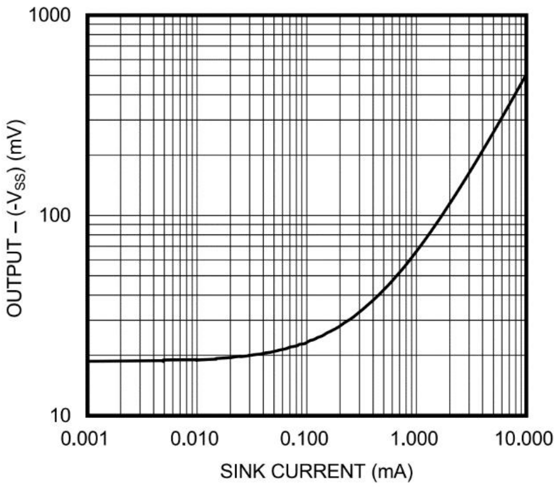


Figure 20. V_{OL} vs. Sink Current

7. DETAILED EXPLANATION

7.1 OUTLINEexplanation

The AD620SQ-CN/883B is a monolithic instrumentation amplifier based on a modification of the classic three op amp approach. Absolute value trimming allows the user to program gain *accurately* with only one resistor. Monolithic construction and laser wafer trimming allow the tight matching and tracking of circuit components, thus ensuring the high level of performance inherent in this circuit.

The internal gain resistors, R1 and R2, are trimmed to an absolute value of 24.7 kΩ, allowing the gain to be programmed accurately with a single external resistor.

$$G = \frac{49.4k\Omega}{R_G} + 1$$

$$R_G = \frac{49.4k\Omega}{G - 1}$$

As a single-ended output from the reference REF pin, the REF pin can be connected to ground or a low-resistance source.

7.2 BLOCK DIAGRAM OF FUNCTIONAL MODULES

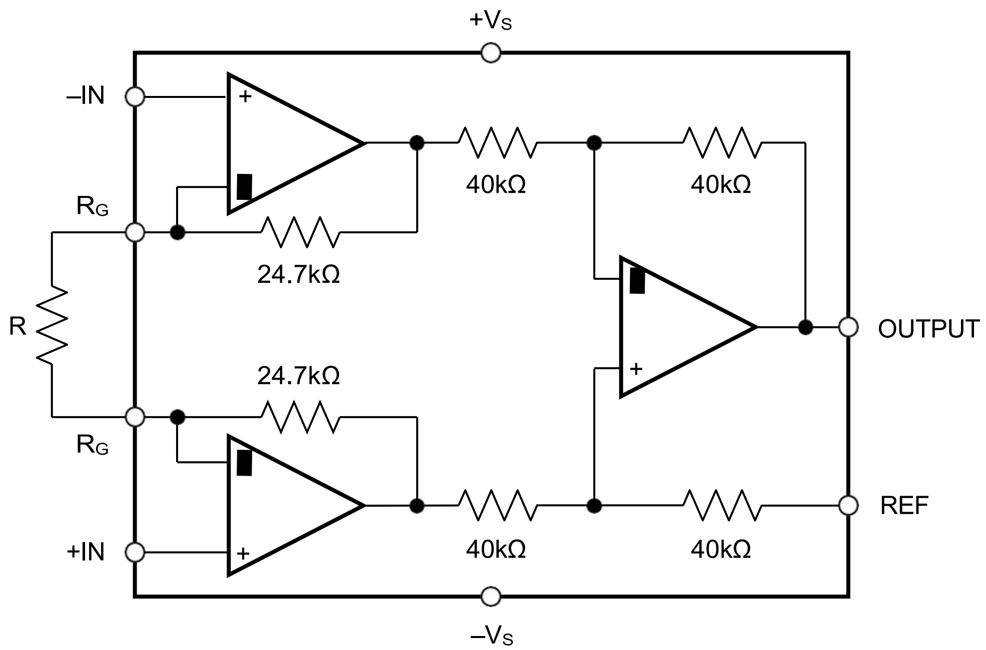


Figure 21. Block Diagram of Functional Modules

7.3 CHARACTERISTIC DESCRIPTION

7.3.1 Gain Selection

The AD620SQ-CN/883B gain is resistor-programmed by R_G, or more precisely, by whatever impedance appears between Pins 1 and 8. The AD620SQ-CN/883B is designed to offer accurate gains using 0.1% to 1% resistors. Table 7 shows required values of R_G for various gains. Note that for G = 1, the R_G pins are unconnected ($R_G = \infty$). For any arbitrary gain, R_G can be calculated by using the formula:

$$R_G = \frac{49.4k\Omega}{G-1}$$

To minimize gain error, avoid high parasitic resistance in series with R_G; to minimize gain drift, R_G should have a low TC —less than 10 ppm/°C—for the best performance.

Table 7. Gain Resistor Selection

1% Std Table Value of R_g (Ω)	Calculated Gain	0.1% Std Table Value of R_g (Ω)	Calculated Gain
49.9k	1.990	49.3k	2.002
12.4k	4.984	12.4k	4.984
5.49k	9.998	5.49k	9.998
2.61k	19.93	2.61k	19.93
1.00k	50.40	1.01k	49.91
499	100.0	499	100.0
249	199.4	249	199.4
100	495.0	98.8	501.0
49.9	991.0	49.3	1,003.0

7.3.2 INPUT AND OUTPUT OFFSET VOLTAGE

The low errors of the AD620SQ-CN/883B are attributed to two sources, input and output errors.
The output error is divided by *G* when referred to the input. In practice, the input errors dominate at high gains, and the output errors dominate at lowgains. The total V_{OS} for a given gain is calculated as:

Total Error RTI = input error + (output error / G)

Total Error RTO = (input error × G) + output error

7.3.3 REFERENCE TERMINAL

The reference terminal potential defines the zero output voltage and is especially useful when the load does not share a precise ground with the rest of the system. It provides a direct means of injecting a precise offset to the output, with an allowable range of 2 V within the supply voltages. Parasitic resistance should be kept to a minimum for optimum CMR.

7.3.4 INPUT PROTECTION

For input voltages beyond the supplies, a protection resistor should be placed in series with each input to limit the current to 10 mA. These can be the same resistors as those used in the RFI filter. High values of resistance can impact the noise and AC CMRR performance of the system. Low leakage diodes (such as the BAV199) can be placed at the inputs to reduce the required protection resistance.

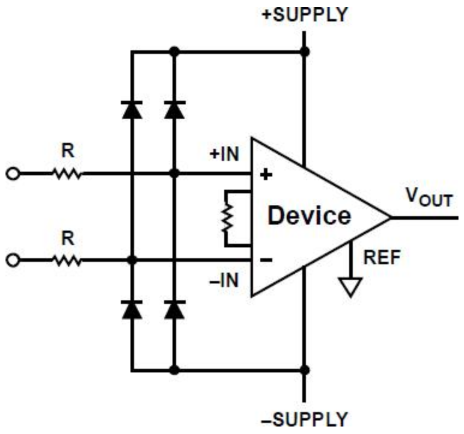


Figure 22. Diode input protection

7.3.5 RF INTERFERENCE

All instrumentation amplifiers rectify small out of band signals. The disturbance may appear as a small dc voltage offset. High frequency signals can be filtered with a low pass R-C network placed at the input of the instrumentation amplifier. Figure 23 demonstrates such a configuration. The filter limits the input signal according to the following relationship:

$$FilterFreq_{DIFF} = \frac{1}{2\pi R(2C_D + C_C)}$$

$$FilterFreq_{CM} = \frac{1}{2\pi RC_C}$$

where $C_D \geq 10C_C$.

C_D affects the difference signal. C_C affects the common-mode signal. Any mismatch in $R \times C_C$ degrades the AD620SQ-CN/883B CMRR.To avoid inadvertently reducing CMRR-bandwidth performance, make sure that C_C is at least one magnitude smaller than C_D. The effect of mismatched C_Cs is reduced with a larger C_D:C_C ratio.

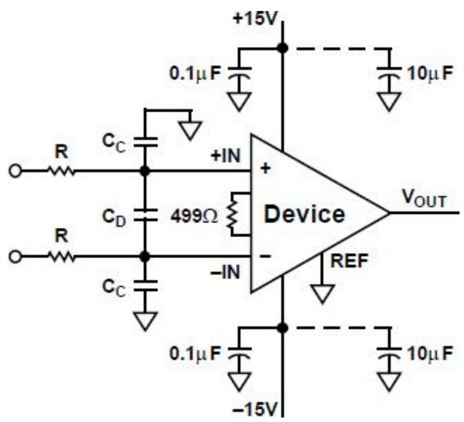


Figure 23. RF Interference Protection

7.3.6 COMMON-MODE REJECTION

Instrumentation amplifiers, such as the AD620SQ-CN/883B, offer high CMR, which is a measure of the change in output voltage when both inputs are changed by equal amounts. These specifications are usually given for a full-range input voltage change and a specified source imbalance.

For optimal CMR, the reference terminal should be tied to a low impedance point, and differences in capacitance and resistance should be kept to a minimum between the two inputs. In many applications, shielded cables are used to minimize noise; for best CMR over frequency, the shield should be properly driven. Figure 24 and Figure 25 show active data guards that are configured to improve ac common-mode rejections by "bootstrapping" the capacitances of input cable shields, thus minimizing the capacitance mismatch between the inputs.

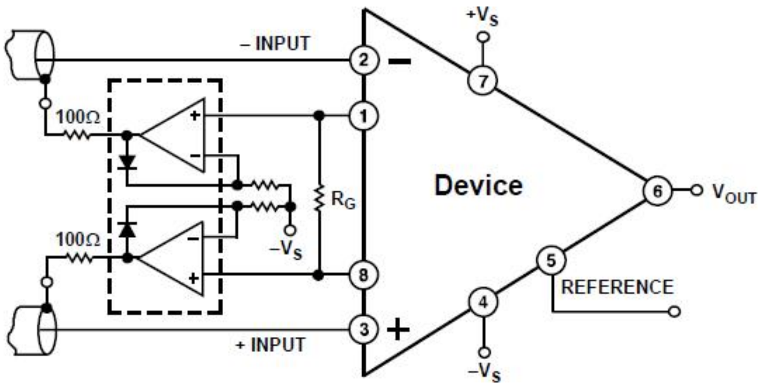


Figure 24. Differential Input Driver

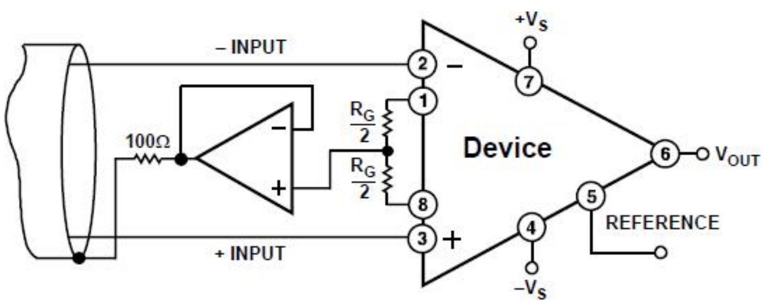


Figure 25. Common-Mode input Driver

7.3.7 GROUND RETURNS FOR INPUT BIAS CURRENTS

Input bias currents are those currents necessary to bias the input transistors of an amplifier. There must be a direct return path for these currents. Therefore, when amplifying "floating" input sources, such as transformers or ac-coupled sources, there must be a dc path from each input to ground, as shown in Figure 26, Figure 27, and Figure 28.

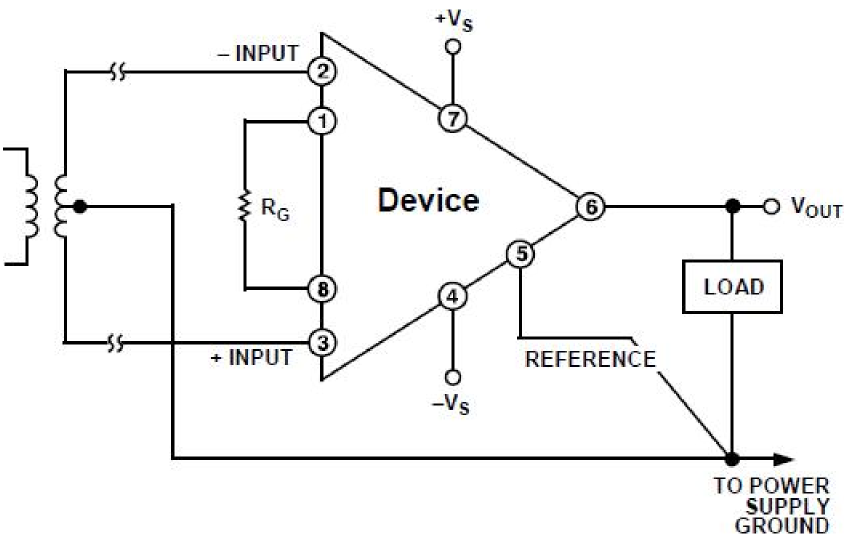


Figure 26. Ground Returns for Bias Currents with Transformer-Coupled Inputs

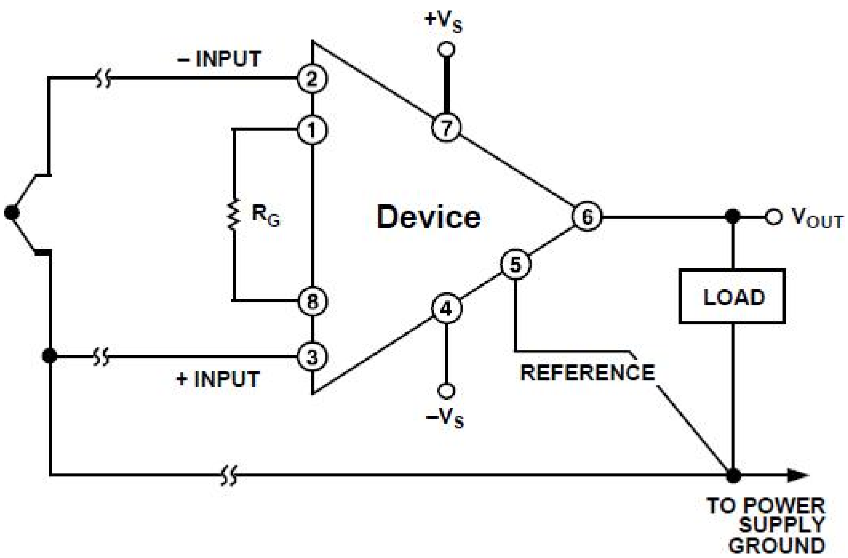


Figure 27. Ground Returns for Bias Currents with Thermocouple Inputs

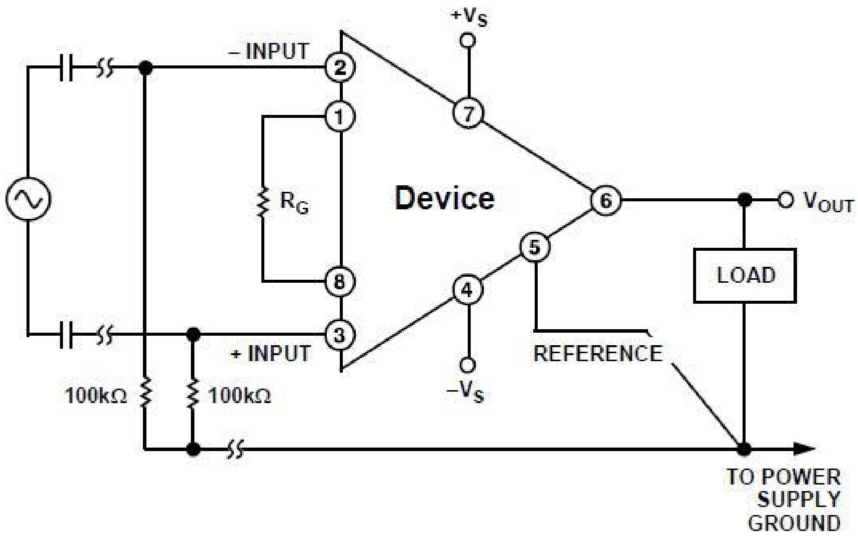


Figure 28. Ground Returns for Bias Currents with AC-Coupled Inputs

8. PACKAGE INFORMATION

SOIC-8 Package

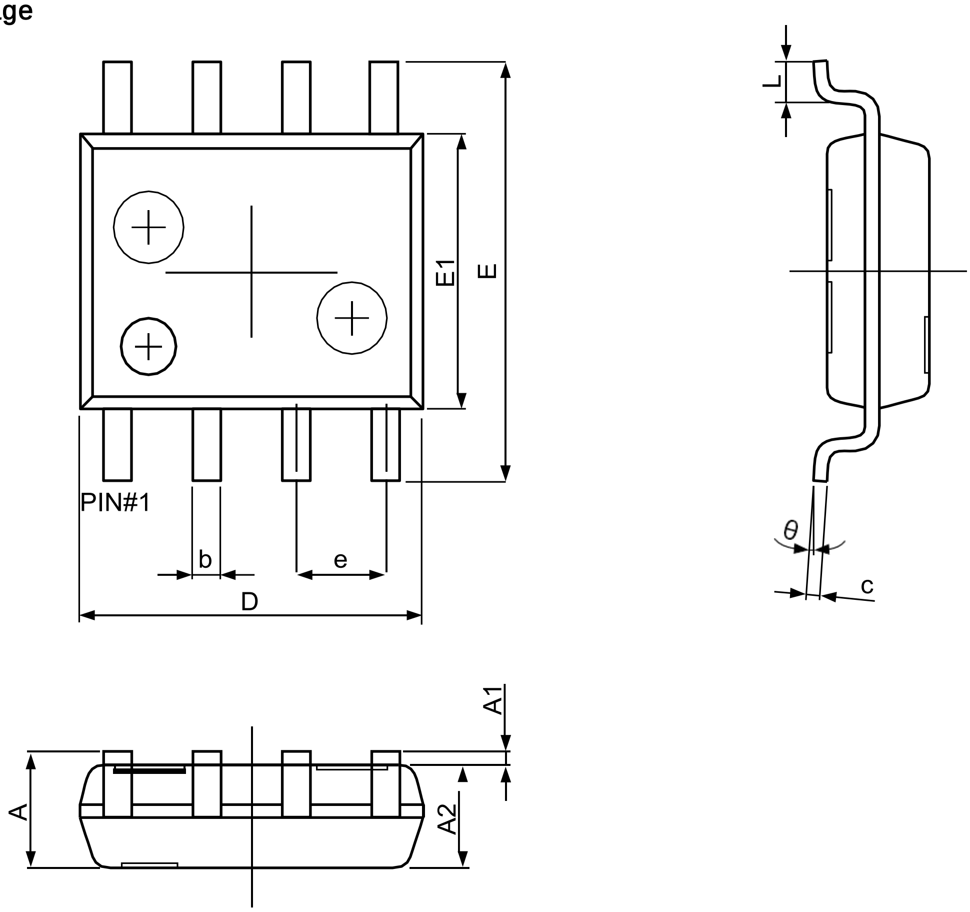


Figure 29. Package View

Table 8 provides detailed information about the dimensions.

Table 8. Dimensions

Symbol	Dimensions in Millimeters		Dimensions in Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.007	0.010
D	4.700	5.100	0.185	0.201
E	5.800	6.200	0.228	0.244
E1	3.800	4.000	0.150	0.157
e	1.270 (BSC)		0.050 (BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

NOTICE

The information presented in this document is for reference only. Involving product optimization and productivity improvement, ChipNobo reserves the right to adjust product indicators and upgrade some technical parameters. ChipNobo is entitled to be exempted from liability for any delay or non-delivery of the information disclosure process that occurs.
本文件中提供的信息仅供参考。涉及产品优化和生产效率改善，ChipNobo 有权调整产品指标和部分技术参数的升级，所出现信息披露过程存在延后或者不能送达的情形，ChipNobo 有获免责权。

The product listed herein is designed to be used with residential and commercial equipment, and do not support sensitive items and specialized equipment in areas where sanctions do exist. ChipNobo Co., Ltd or anyone on its behalf, assumes no responsibility or liability for any damages resulting from improper use.
此处列出的产品旨在民用和商业设备上使用，不支持确有制裁地区的敏感项目和特殊设备，ChipNobo 有限公司或其代表，对因不当使用而造成的任何损害不承担任何责任。

For additional information, please visit our website https://www.chipnobo.com/en or consult your nearest Chipnobo sales office for further assistance.
欲了解更多信息，请访问我们的网站 https://www.chipnobo.com/en，或咨询离您最近的 Chipnobo 销售办事处以获得进一步帮助。