General Description

The TLV76733DRVR-CN is a low-dropout (LDO) voltage regulator offering the benefits of wide input voltage range, low dropout voltage, low power consumption, and miniaturized packaging.Quiescent current of only 1.5uA makes this device ideal for powering the battery-powered, always-on systems that require very little idle-state power dissipation to a longer service life.There is a shutdown mode by pulling the EN pin low. The shutdown current in this mode goes down to only 100nA (typical).The TLV76733DRVR-CN of linear regulator is stable with the ceramic output capacitor over its wide input range from 2V to 24V and the entire range of output load current (0mA to 500mA).

Features

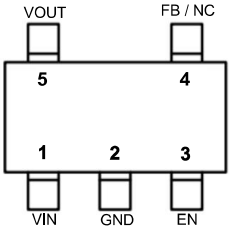
- 1.5μA Ground Current at no Load
- ±1% Output Accuracy
- 500mA Output Peak Current
- 100nA Disable Current
- Wide Operating Input Voltage Range: 2V to 24V
- Dropout Voltage: 0.35V at 100mA / V_{OUT} 5V
- Support Fixed Output Voltage 1.8V, 3.3V, 5V
- Adjustable Output Voltage Available by Specific Application
- Stable with Ceramic or Tantalum Capacitor
- Current Limit Protection
- Over-Temperature Protection
- SOT-23-5 Package Available

Applications

- Portable, Battery Powered Equipment
- Low Power Microcontrollers
- Laptop, Palmtops and PDAs
- Wireless Communication Equipment
- Audio/Video Equipment
- Car Navigation Systems
- Industrial Controls
- Weighting Scales
- Meters
- Home Automation

Pin Configurations

SOT-23-5



Ordering Information

Description	Symbol	Description
Output Voltage	18	V_{OUT} = 1.8V
	..	..
	..	..
	33	V_{OUT} = 3.3V
	50	V_{OUT} = 5.0V
Package type	M5	SOT-23-5

Special Request : Any Voltage between 1.8V and 5V under specific business agreement.

Description of Functional Pins

Pin No	Pin Name	Pin Function
TLV76733DRVR-CN		
1	VIN	Input of Supply Voltage
2	GND	Ground
3	EN	Enable Control Input
4	NC	No internal connection
	FB	Feedback input
5	VOUT	Output of the Regulator

Typical Application Circuits

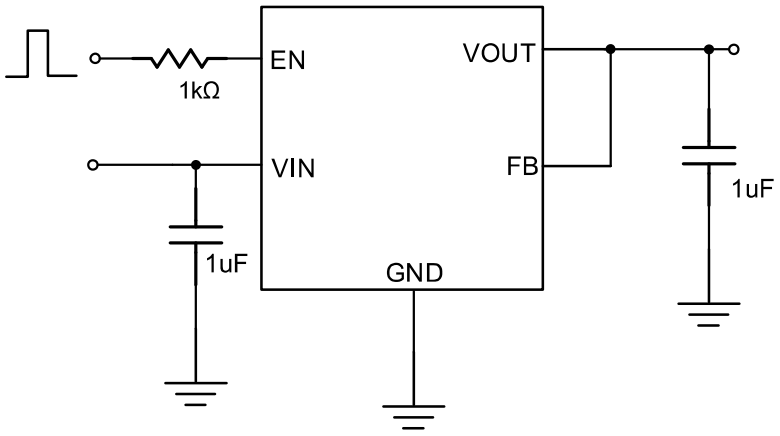


Figure 1: Application circuit of Fixed V_{OUT} LDO with enable and sense functions

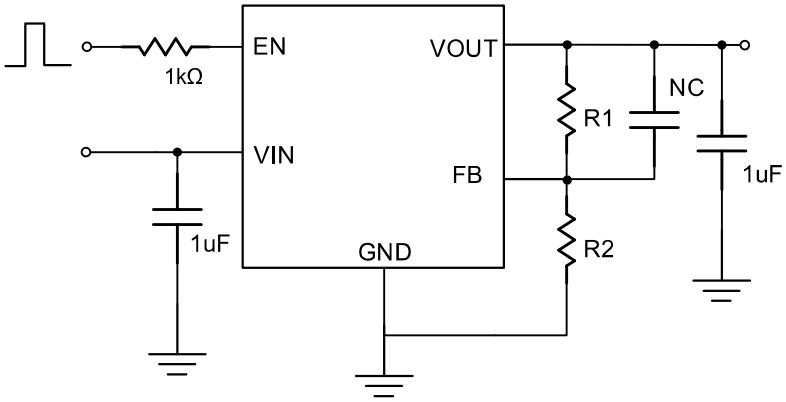


Figure 2: Adjustable output voltage LDO application circuit

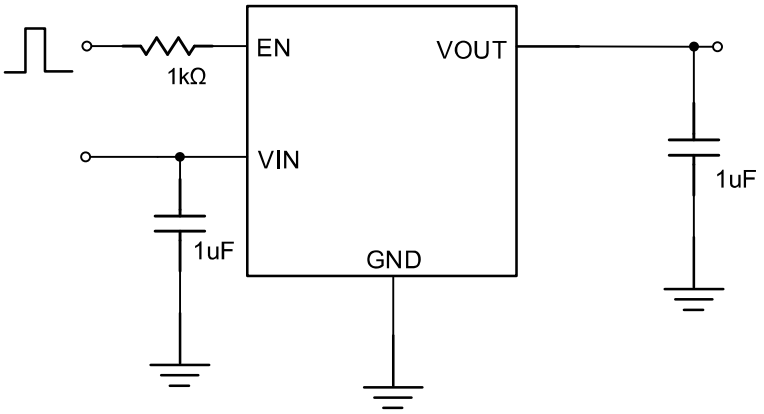
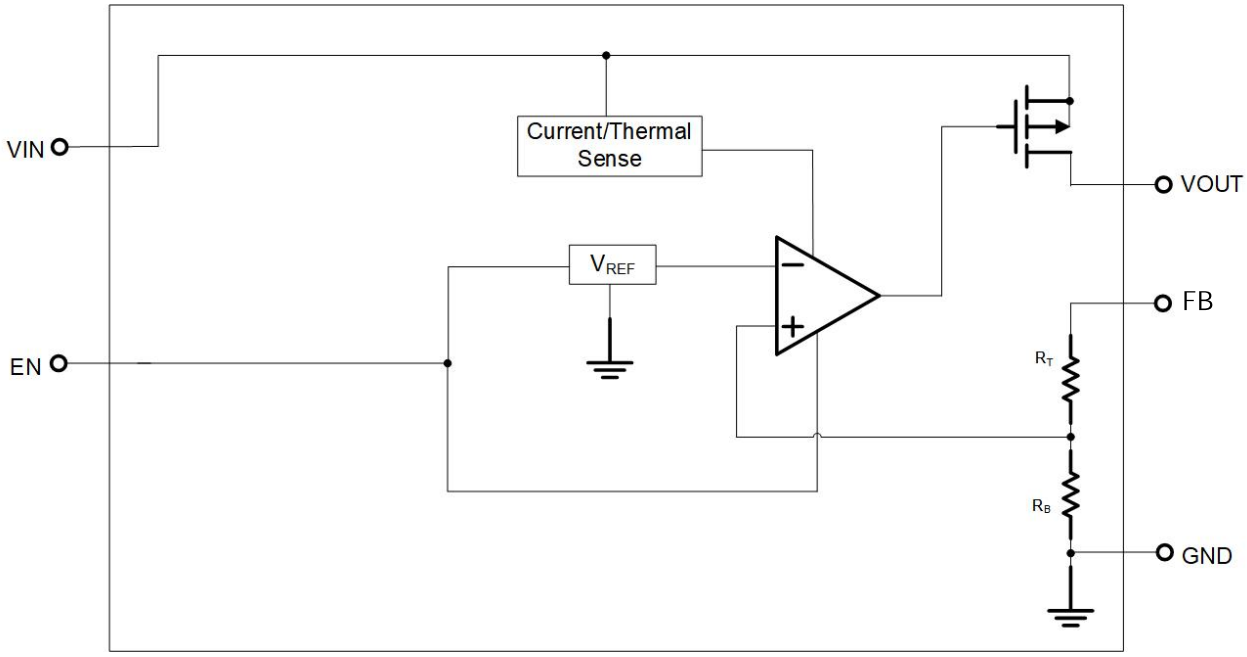


Figure 3: Application circuit of Fi xed VOUT LDO with enable function

Function Block Diagram



Absolute Maximum Ratings (Note 1)

VIN, EN to GND ---------- -0.3V to 30V

FB to GND ---------- -0.3V to 6V

VOUT to GND

HL64S18, HL64S33, HL64S50 ---------- -0.3V to 6V

VOUT to VIN ---------- -28V to 0.3V

Package Thermal Resistance (Note 2)

SOT-23-5, θ_{JA} ---------- 220 °C /W

Lead Temperature (Soldering, 10 sec.) ---------- 260 °C

Junction Temperature ---------- 150 °C

Storage Temperature Range ---------- -40 °C to 150 °C

ESD Susceptibility

HBM ---------- 2KV

MM ---------- 200V

Recommended Operating Conditions

Input Voltage VIN ---------- 2.0V to 24V

Junction Temperature Range ---------- -40 °C to 125 °C

Ambient Temperature Range ---------- -40 °C to 85 °C

Electrical Characteristics

(V_{IN} =12V, V_{EN} =5V, T_A=25°C unless otherwise specified)

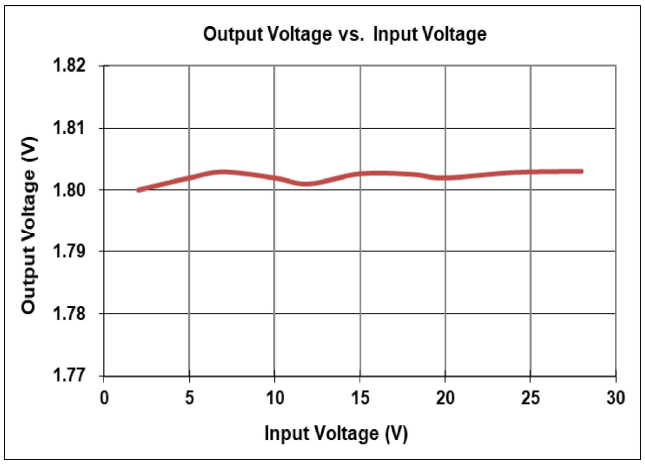
Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage	V_{IN}		2	--	24	V
DC Output Voltage Accuracy		I_{LOAD} = 0.1mA	-1		1	%
Dropout Voltage (I_{LOAD} =100mA)	V_{DROP}	V_{OUT} ≥ 5V	--	0.35		V
	$V_{DROP\_3.3V}$	V_{OUT} = 3.3V		0.42		
	$V_{DROP\_1.8V}$	V_{OUT} = 1.8V		0.5		
Ground Current (I_{LOAD} = 0mA) (Note 3)	I_Q	V_{IN} > V_{OUT}		1.5		μA
Shutdown Ground Current	I_{SD}	V_{EN} = 0V, V_{OUT} = 0V		0.1	0.5	μA
FB Input Current	I_{FB}	FB = V_{OUT} V_{OUT} ≤ 5V		0.7		μA
Enable Threshold Voltage	V_{IH}	EN Rising	1.1			V
	V_{IL}	EN Falling			0.4	
EN Input Current	I_{EN}	V_{EN} = 24V		10	100	nA
Line Regulation	ΔLINE	I_{LOAD} = 1mA, 10V ≤ V_{IN} ≤ 20V	--	0.5		%
Load Regulation	ΔLOAD	10mA ≤ I_{LOAD} ≤ 0.2A		0.3		%
Output Peak Loading Current	I_{OUT}	V_{IN} = V_{OUT} + 1.8V		500		mA
Output Current Limit	I_{LIM}	V_{OUT} = 0V	501	700		mA
Power Supply Rejection Ratio	PSRR	V_{OUT} = 5V, I_{LOAD} = 30mA, V_{IN} = 12V, f = 1KHz		70		dB
Thermal Shutdown Temperature	T_{SD}	I_{LOAD} = 10mA	--	160	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}			15		°C

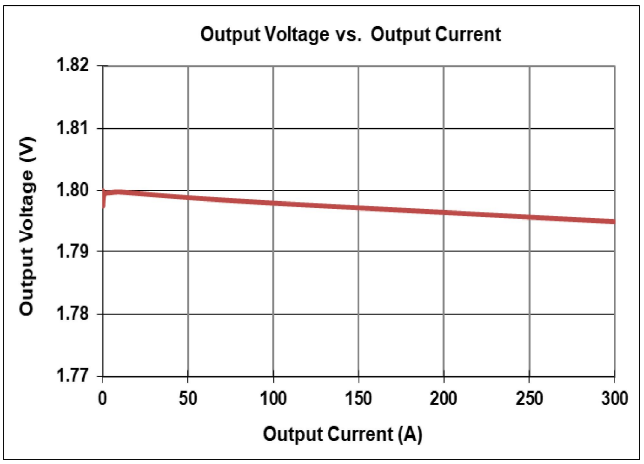
Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

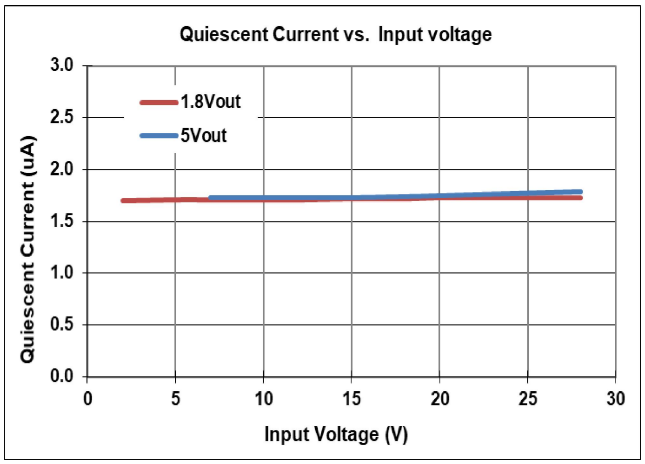
Note 2. θ_{JA} is measured at T_A = 25°C on a DSTECH EVB board.

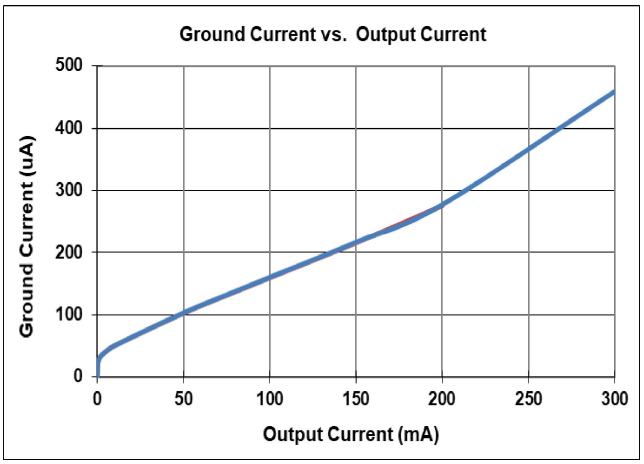
Note 3. When V_{IN} > V_{OUT}, the quiescent current is the normal specification value, but when V_{IN} ≤ V_{OUT}, the quiescent current will be greater than the specification value.

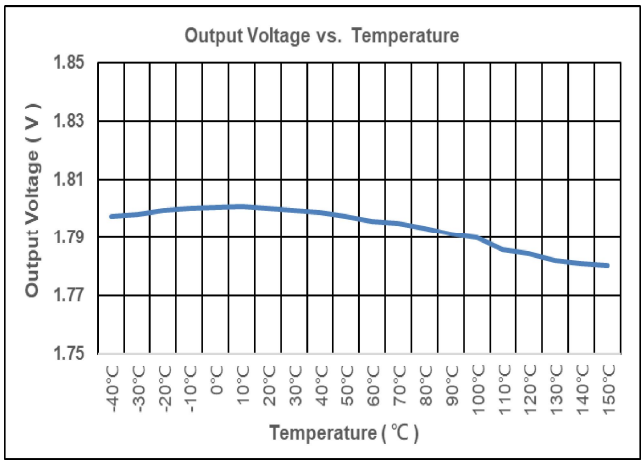
Typical Characteristics

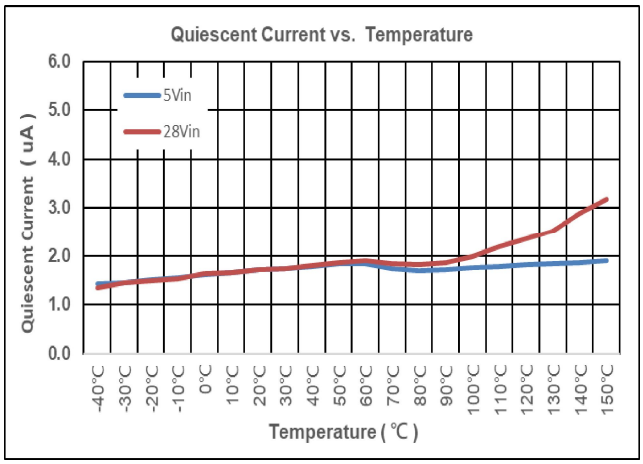


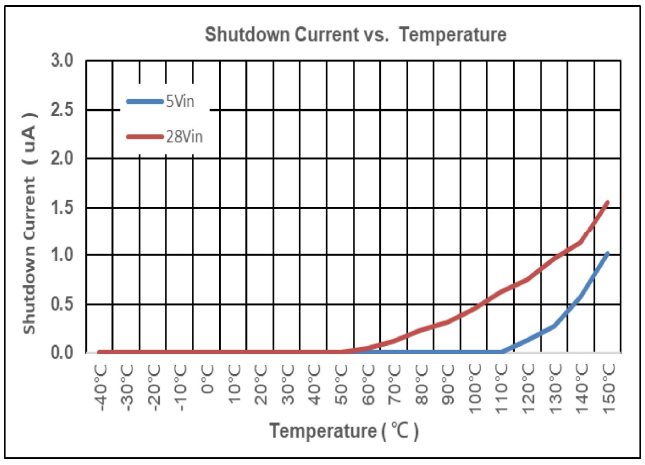


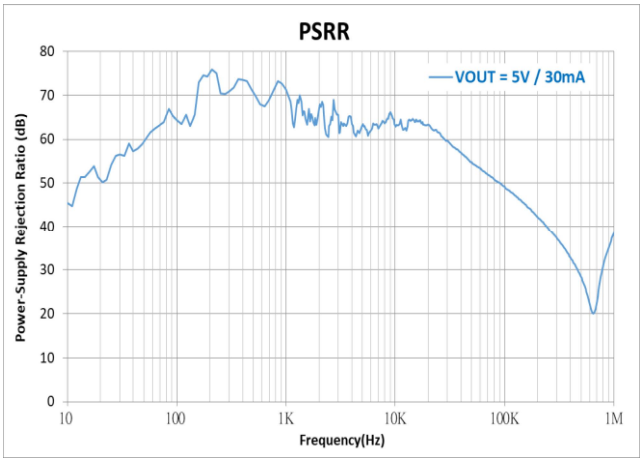





Output Voltage vs. Temperature
Output Voltage (V)
1.85
1.83
1.81
1.79
1.77
1.75
-40°C -30°C -20°C -10°C 0°C 10°C 20°C 30°C 40°C 50°C 60°C 70°C 80°C 90°C 100°C 110°C 120°C 130°C 140°C 150°C
Temperature (℃)


Quiescent Current vs. Temperature
Quiescent Current (uA)
6.0
5.0
4.0
3.0
2.0
1.0
0.0
5Vin
28Vin
-40°C -30°C -20°C -10°C 0°C 10°C 20°C 30°C 40°C 50°C 60°C 70°C 80°C 90°C 100°C 110°C 120°C 130°C 140°C 150°C
Temperature (℃)


Shutdown Current vs. Temperature
Shutdown Current (uA)
3.0
2.5
2.0
1.5
1.0
0.5
0.0
5Vin
28Vin
-40°C -30°C -20°C -10°C 0°C 10°C 20°C 30°C 40°C 50°C 60°C 70°C 80°C 90°C 100°C 110°C 120°C 130°C 140°C 150°C
Temperature (℃)


PSRR
Power-Supply Rejection Ratio (dB)
80
70
60
50
40
30
20
10
0
VOUT = 5V / 30mA
10
100
1K
10K
100K
1M
Frequency(Hz)

Application Guideline

Input and Output Capacitor Requirements

The external input and output capacitors of TLV76733DRVR-CN must be propery selected for stability and performance. Use a 1uF or larger input capacitor and place it close to the lC's VIN and GND pins.Any output capacitor meeting the minimum 1mΩ ESR (Equivalent Series Resistance) and effective capacitance between 1uF and 22uF requirement may be used. Place the output capacitor close to the IC's VOUT and GND pins.Increasing capacitance and decreasing ESR can improve the circuit's PSRR and line transient response.

Current Limit

The TLV76733DRVR-CN contains the current limiter of output power transistor, which monitors and controls the transistor, limiting the output current to 700mA (typical). The output can be shorted to ground indefinitely without damaging the part.

Dropout Voltage

The TLV76733DRVR-CN uses a PMS pass transistor to achieve low dropout. When (VIN- VOUT) is less than the dropout voltage (V_{DROP}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the RDS(ON) of the PMOS pass element. V_{DROP} scales approximately with the output current because the PMOS device behaves as a resistor in dropout condition.

As any linear regulator, PSRR and transient response are degraded as (VIN-VOUT)approaches dropout condition.

Adjustable Output Voltage Application

The TLV76733DRVR-CN with FB pin also can work as an adjustable output voltage LDO. Figure 2 gives the connections for the adjustable output voltage application.The resistor divider from VOUT to FB sets the output voltage when in regulation.

The voltage on the FB pin sets the output voltage and is determined by the values of R1 and R2. In order to keep a good temperature coefficient of output voltage, the values of R1 and R2 should be selected carefully to ignore the temperature effect of input current at the FB pin.A current greater than 50μA in the resistor divider is recommended to meet the above requirement.The adjustable output voltage can be calculated using the formula given in equation 1:

$$V_{OUT} = \frac{R1+R2}{R2} \times V_{FB} \quad (1)$$

OTP (Over Temperature Protection)

The over temperature protection function of TLV76733DRVR-CN will turn off the P-MOSFET when the junction temperature exceeds 160°C(typ.). Once the junction temperature cools down by approximately 15°C, the regulator will automatically resume operation.

Thermal Application

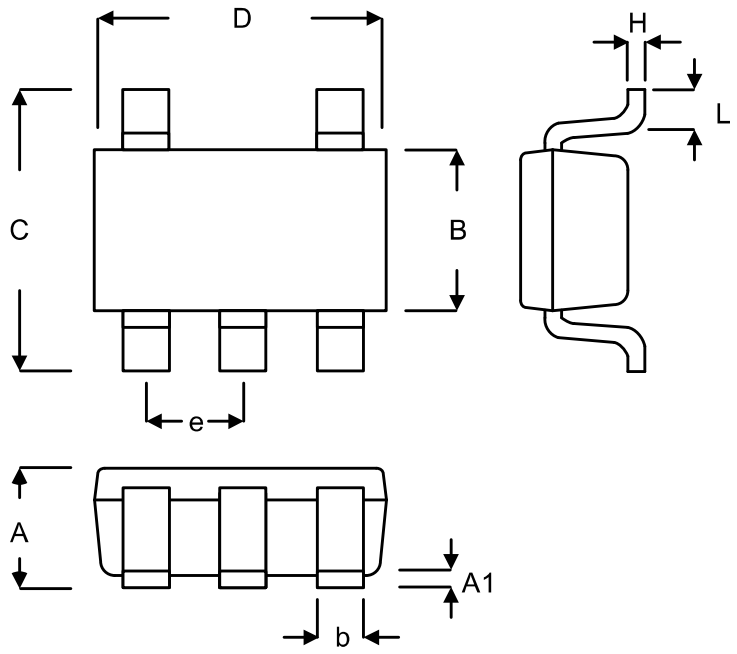
For continuous operation, do not exceed the absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated as below:

TA=25°C, DSTECH PCB,
The max PD (Max)=(125°C-25°C)/(220°C/)=0.45W for SOT-23-5 packages.
Power dissipation (PD)is equal to the product of the output current and the voltage drop across the output pass element, as shown in the equation below:
PD =(VIN-VOUT)xIOUT

Layout Consideration

By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the TLV76733DRVR-CN ground pin using as wide and as short of a copper trace as is practical. Connections using long trace lengths, narrow trace widths, and/or connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

Package Information:



Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.250	0.560	0.010	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

SOT-23-5L

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