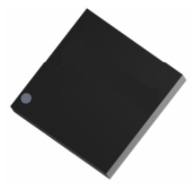
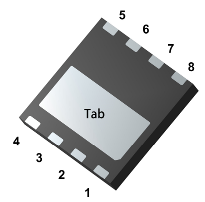
1. Description

The TP65H070G4LSGB-TR-CN series FETs are hybrid normally-off Gallium Nitride (GaN) field effect transistors with the strongest gate and the lowest reverse voltage drop of all wide-band-gap devices in the market. They allow simple gate drive, offer best-in-class performance and outstanding reliability.

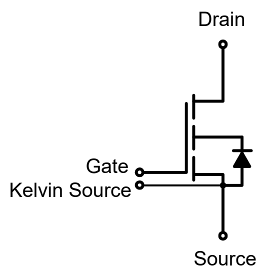


Top View



Bottom View

Source	1, 2, Tab
Kelvin Source	3
Gate	4
Drain	5, 6, 7, 8



Schematic Symbol

Features

- Strong gate with a high threshold, no need for negative gate drive, and a high repetitive input voltage tolerance of ±20V.
- Fast turn-on/off speed for reduced cross-over losses.
- Low Q_g and simple gate drive for lowest driver consumption at high frequencies.
- Lowest V_F in off-state reverse conduction among all SiC and GaN FETs for low loss during dead-times.
- Low Q_{rr} for outstanding hard-switched bridge applications.
- High spike tolerance of 800V for enhanced reliability.

Benefits

- Enable very high conversion efficiencies.
- Enable higher frequency for compact power supplies.
- End-product cost & size savings due to reduced cooling requirements.
- Improved safety & reliability due to cooler operation temperature.

Applications

- Half-bridge buck/boost, totem-pole PFC circuits or inverter circuits.
- High-efficiency/High-frequency LLC or other soft-switching topologies.

Key Performance Parameters	
V_{DSS} (V)	650
$V_{DSS(PK), nonrepetitive}$ (V) [a)]	800
$V_{DSS(PK), repetitive}$ (V) [b)]	750
$R_{DS(on), typ}$ (mΩ) [c)]	92
Q_{oss} (nC)	55.6
Q_g (nC)	14.4

[a)] Duty < 1%, spike duration < 30µs, nonrepetitive
[b)] Duty < 1%, spike duration < 30µs, repetitive
[c)] Dynamic on-resistance

Part Number & Package Information

Part #	Package	Package Base
TP65H070G4LSGB-TR-CN	DFN 8x8 (mm)	Source

2. Maximum Ratings

Symbol	Parameter	Value
V_{DSS} (V)	Drain-source maximum voltage (T_J = -55°C to 150°C)	650
$V_{DSS(PK), nonrepetitive}$ (V)	Drain-source maximum peak voltage, nonrepetitive [a)]	800
$V_{DSS(PK), repetitive}$ (V)	Drain-source maximum peak voltage, repetitive [a)]	750
V_{GSS} (V)	Gate-source maximum voltage	±20
P_D (W)	Maximum power dissipation (T_C = 25°C)	65.8
I_{DS} (A)	Maximum continuous drain current (T_C = 25°C)	18.9
	Maximum continuous drain current (T_C = 100°C)	12
$I_{DS (pulse)}$ (A)	Maximum pulse drain current (T_C = 25°C) [b)]	95
T_J (°C)	Operating junction temperature	-55 to +150
T_S (°C)	Storage temperature	-55 to +150
T_{sold} (°C)	Reflow soldering temperature [c)]	260

[a)] Duty cycle < 1%, spike duration < 30µs
[b)] Pulse width = 10µs
[c)] Reflow MSL3

3. Thermal Characteristics

Symbol	Parameter	Typ.
$R_{\Theta JC}$ (°C/W)	Junction-to-case thermal resistance	1.9
$R_{\Theta JA}$ (°C/W)	Junction-to-ambient thermal resistance [a)]	50

[a)] Soldered on a PCB of 6cm^2 metal area and 70µm thickness

4. Device Characteristics T_J = 25°C unless specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{DSS}	Drain-source maximum voltage	650	-	-	V	V_{GS} = 0V
$V_{GS(th)}$	Gate threshold voltage	3.2	3.65	4.1	V	V_{DS} = V_{GS}, I_D = 1.8mA
$R_{DS(on)}$	Drain-source on resistance [a]	-	92	110	mΩ	V_{GS} = 10V, I_D = 12A
		-	184	-	mΩ	V_{GS} = 10V, I_D = 12A, T_J = 150°C
I_{DSS}	Drain-source leakage current	-	2.5	25	µA	V_{DS} = 650V, V_{GS} = 0V
		-	5	-	µA	V_{DS} = 650V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-source leakage current	-	-	100	nA	V_{GS} = 20V
		-	-	-100	nA	V_{GS} = -20V
C_{iss}	Input capacitance	-	818	-	pF	V_{GS} = 0V, V_{DS} = 400V, *f* = 500kHz
C_{oss}	Output capacitance	-	53	-	pF	V_{GS} = 0V, V_{DS} = 400V, *f* = 500kHz
C_{rss}	Reverse transfer capacitance	-	3.6	-	pF	V_{GS} = 0V, V_{DS} = 400V, *f* = 500kHz
$C_{o(er)}$	Equivalent output capacitance (energy related)	-	78	-	pF	V_{GS} = 0V, V_{DS} = 0V to 400V
$C_{o(tr)}$	Equivalent output capacitance (time related)	-	139	-	pF	V_{GS} = 0V, V_{DS} = 0V to 400V
Q_g	Gate charge total	-	14.4	-	nC	V_{DS} = 400V, V_{GS} = 0V to 10V, I_D = 12A
Q_{gs}	Gate to source charge	-	4.7	-	nC	
Q_{gd}	Gate to drain charge	-	5.2	-	nC	
Q_{oss}	Output charge	-	55.6	-	nC	V_{GS} = 0V, V_{DS} = 0V to 400V
$t_{d(on)}$	Turn-on delay time	-	23	-	ns	V_{DS} = 400V, V_{GS} = 0V to 12V, I_D = 13A, R_G = 36Ω, Z_{FB} = 120Ω @100MHz, see Figure 13
t_r	Rise time	-	7.1	-	ns	
$t_{d(off)}$	Turn-off delay time	-	58	-	ns	
t_f	Fall time	-	7.5	-	ns	

[a] Dynamic on-resistance

Reverse Device Characteristics, T_J = 25°C unless specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
I_S	Reverse current	-	-	12	A	V_{GS} = 0V, T_C = 100°C, ≤ 25% duty cycle
$I_{S\,(pulse)}$	Reverse pulse current	-	-	35	A	V_{GS} = 0V, V_{SD} = 6V, pulse width ≤ 10µs, T_J = 150°C
V_{SD}	Reverse voltage [a]	-	1.7	-	V	V_{GS} = 0V, I_S = 12A
		-	1.4	-	V	V_{GS} = 0V, I_S = 8A
t_{rr}	Reverse recovery time	-	17.9	-	ns	I_S = 13A, V_{DD} = 400V, di/dt = 1000A/µs
Q_{rr}	Reverse recovery charge [b]	-	<2.5	-	nC	

[a] Including the effect of dynamic on-resistance
[b] Excluding Q_{oss}

5. Typical Characteristics (T_C = 25°C unless specified)

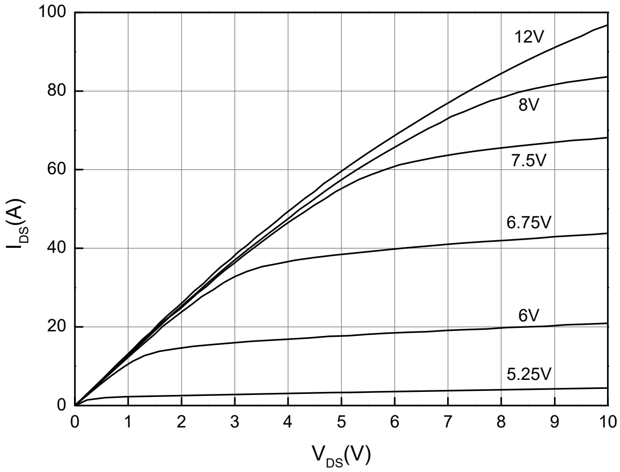


Figure 1. Typical Output Characteristics at T_J = 25°C (Parameter: V_{GS})

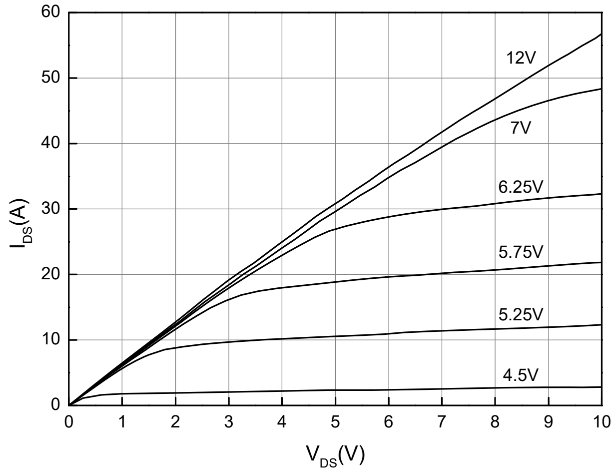


Figure 2. Typical Output Characteristics at T_J = 150°C (Parameter: V_{GS})

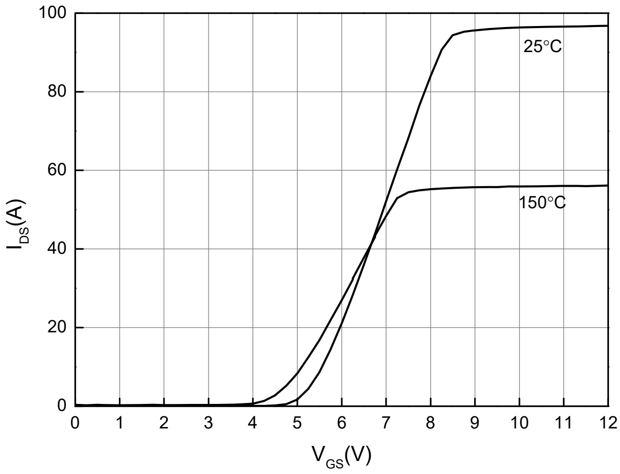


Figure 3. Typical Transfer Characteristics (V_{DS} = 10V, Parameter: T_J)

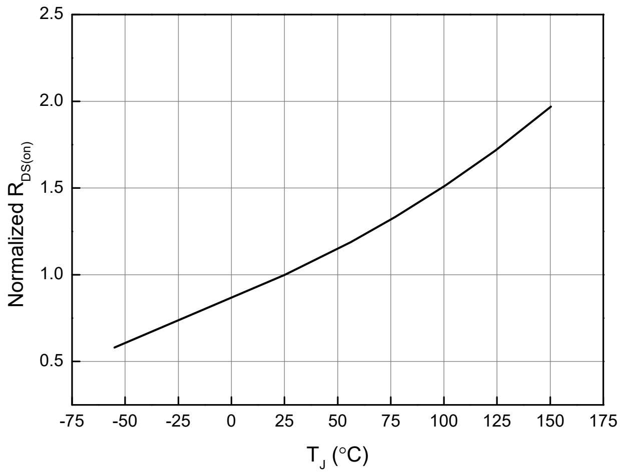


Figure 4. Normalized On-Resistance (I_D = 12A, V_{GS} = 10V)

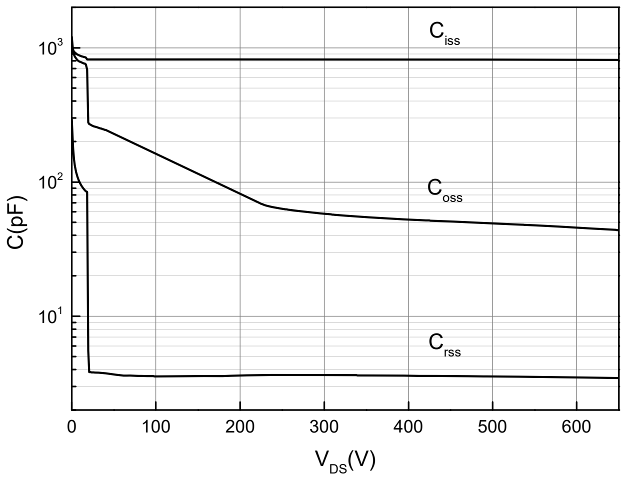


Figure 5. Typical Capacitance
(V_{GS} = 0V, *f* = 500kHz)

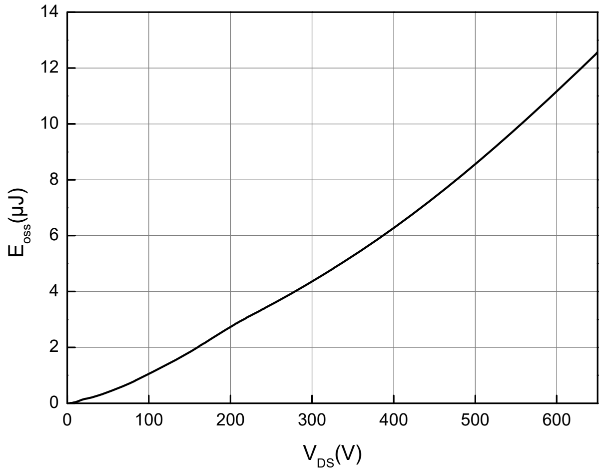


Figure 6. Typical C_{oss} Stored Energy

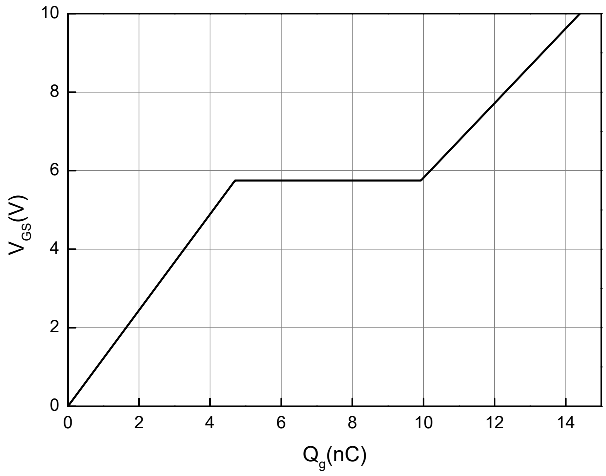


Figure 7. Typical Gate Charge
(I_{DS} = 12A, V_{DS} = 400V)

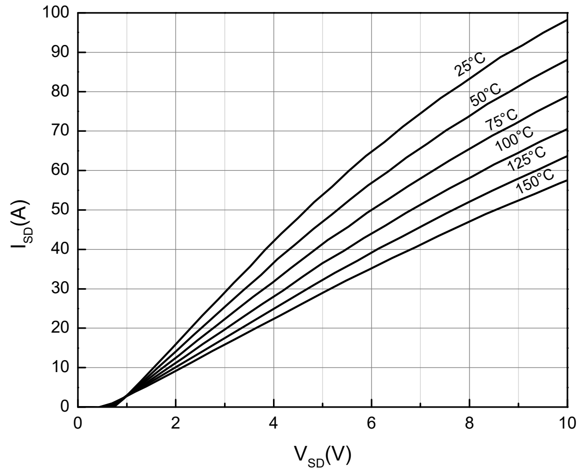


Figure 8. Reverse Conduction Characteristics
(-20V ≤ V_{GS} ≤ 0V, Parameter: T_J)

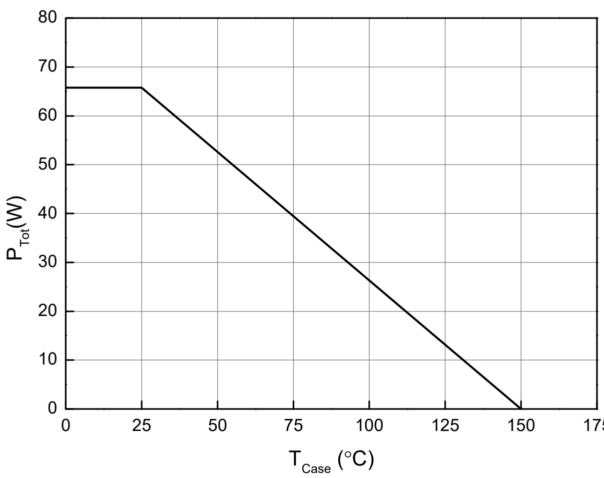


Figure 9. Power Dissipation

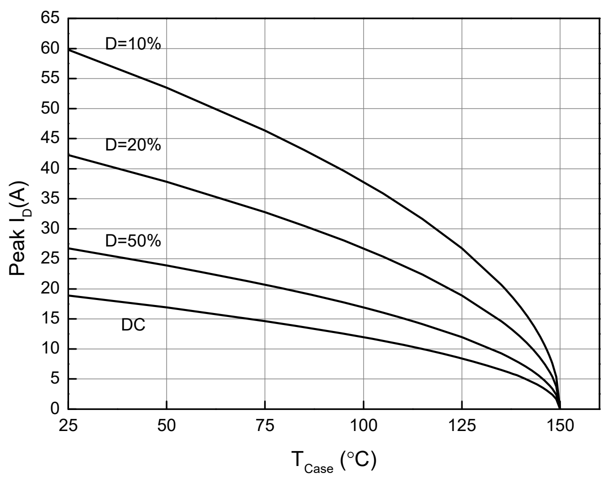


Figure 10. Current Derating
(Pulse Width ≤ 10μs, V_{GS} ≥ 10V)

6. Design Considerations

The fast switching of GaN device reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

DO	DO NOT
Place gate driver close to the GaN device and separate input traces from output traces	Use long gate drive traces, long lead length and route the output traces next to the input
Use gate ferrite bead and dc-link RC snubber	Use close-by decoupling capacitor without series resistor
Minimize trace length of the PCB layout for both drive loop and power loop	Use a traditional differential voltage probe for V_{gs} of high side device

7. Circuit Implementation

Half-bridge Schematic

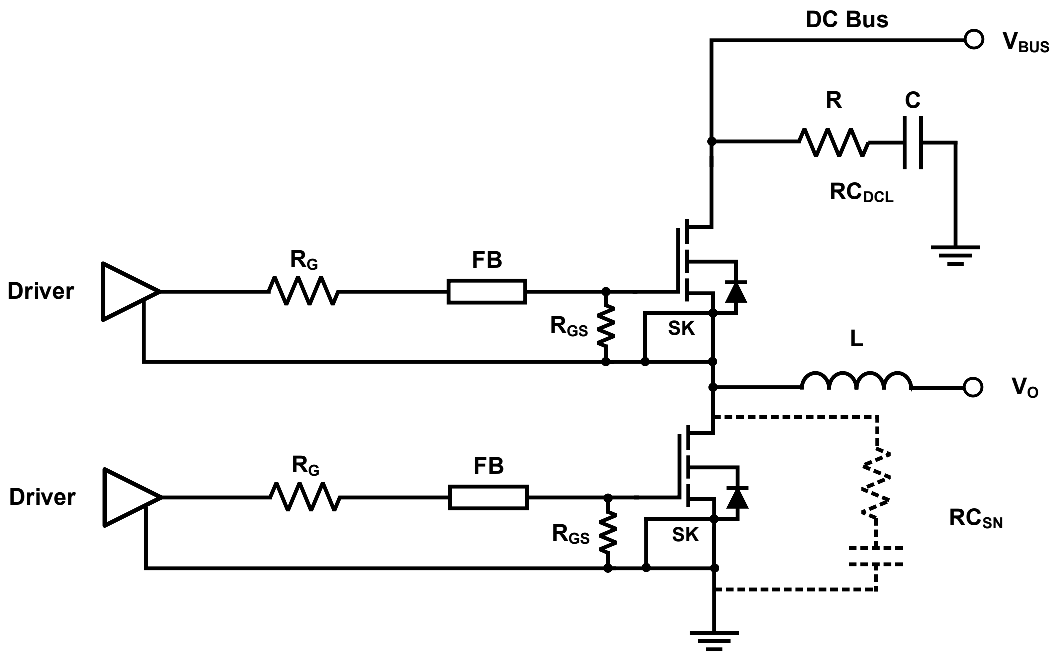


Figure 13. Simplified half-bridge schematic

Recommended gate drive: (0V, 10-12V) with R_G = 36Ω [a)]

Gate Ferrite Bead (FB) [b)]	Required DC Link RC Snubber (RC_{DCL}) [c)]	Recommended Switching Node RC Snubber (RC_{SN})
100-330Ω@100MHz	(10nF+10Ω) × 2	Not necessary, see note **d** and **e** below

Notes:

a) For bridge topologies only. R_G could be smaller in single ended topologies.

b) Examples of material selection: MPZ2012S***AT000(TDK), BLM21PG***SZ1D(Murata).

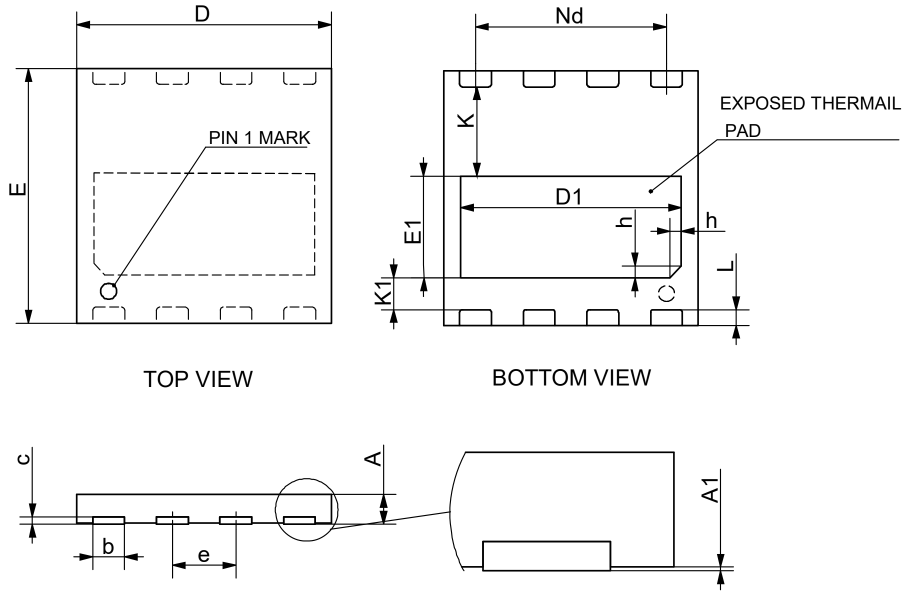
c) RC_{DCL} should be placed as close as possible to the drain pin. Other decoupling capacitors should be located away from the RC_{DCL}.

d) RC_{SN} is needed only if R_G is smaller than recommendations.

e) If required, please use 15Ω+68pF.

f) The typical value of R_{GS} is 10kΩ.

8. Package Dimensions

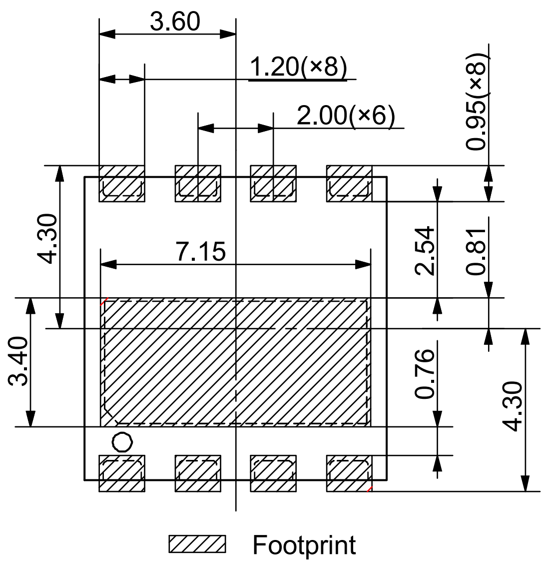


TOP VIEW BOTTOM VIEW

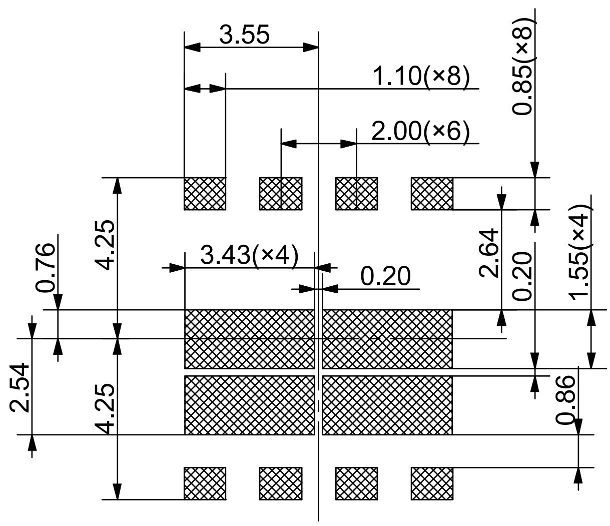
SIDE VIEW

DIM.	Millimeters		
	MIN.	TYP.	MAX.
A	1.05	1.10	1.15
A1	0.00	0.02	0.05
b	0.90	1.00	1.10
c	-	0.20	-
D	7.90	8.00	8.10
D1	6.85	6.95	7.05
E	7.90	8.00	8.10
E1	3.10	3.20	3.30
e	2.00 BSC		
Nd	6.00 BSC		
h	0.15	0.25	0.35
K	2.70	2.80	2.90
K1	0.90	1.00	1.10
L	0.40	0.50	0.60
DFN 8×8 (TP65H070G4LSGB-TR-CN)			
Date:2022.5	Rev. 01		
Lead finish: Sn Plating			

9. Recommended PCB Land Pattern



TOP VIEW



TOP VIEW

Recommended stencil apertures
(Based on stencil thickness of 0.130 mm)

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