

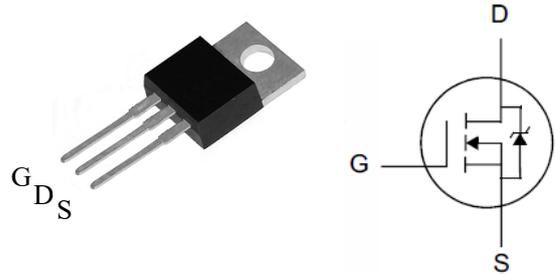
General Features

- Proprietary New Trench Technology
- $R_{DS(ON),typ.}=3.4m\Omega@V_{GS}=10V$
- Low on-resistance $R_{DS(ON)}$
- 150°C operating temperature

BV_{DSS}	$R_{DS(ON),typ.}$	I_D
100V	3.4mΩ	175A

Applications

- DC/DC Converter
- Motor control and drive
- Battery management
- Synchronous Rectification
- Switching Power



TO-220

Package No to Scale

Ordering Information

Part Number	Package
IRFB4110PBF-CN	TO-220

Absolute Maximum Ratings

$T_c=25^\circ C$ unless otherwise specified

Symbol	Parameter	IRFB4110PBF-CN	Unit
V_{DSS}	Drain-to-Source Voltage	100	V
V_{GSS}	Gate-to-Source Voltage	±20	
I_D	Continuous Drain Current	175	A
	Continuous Drain Current @ $T_c=100^\circ C$	122	
I_{DM}	Pulsed Drain Current at $V_{GS}=10V$	500	
E_{AS}	Single Pulse Avalanche Energy ^[3]	1000	mJ
P_D	Power Dissipation	227	W
	Derating Factor above 25°C	1.81	W/°C
T_L	Soldering Temperature Distance of 1.6mm from case for 10 seconds	300	°C
T_J & T_{STG}	Operating and Storage Temperature Range	-55 to 150	

Caution: Stresses greater than those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device.

Thermal Characteristics

Symbol	Parameter	IRFB4110PBF-CN	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.55	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	62	

Electrical Characteristics

OFF Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	100	--	--	V	$V_{GS}=0V, I_D=250\mu A$
I_{DSS}	Drain-to-Source Leakage Current	--	--	1	μA	$V_{DS}=100V, V_{GS}=0V$
I_{GSS}	Gate-to-Source Leakage Current	--	--	+100	nA	$V_{GS}=+20V, V_{DS}=0V$
		--	--	-100		$V_{GS}=-20V, V_{DS}=0V$

ON Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	--	3.4	4.0	m Ω	$V_{GS}=10V, I_D=50A$
$V_{GS(TH)}$	Gate Threshold Voltage	2.2	--	3.8	V	$V_{DS}=V_{GS}, I_D=250\mu A$

Dynamic Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
C_{iss}	Input Capacitance	--	6996	--	pF	$V_{GS}=0V, V_{DS}=50V, f=1.0MHz$
C_{rss}	Reverse Transfer Capacitance	--	48	--		
C_{oss}	Output Capacitance	--	925	--		
Q_g	Total Gate Charge	--	128	--	nC	$V_{DD}=50V, I_D=50A, V_{GS}=0 \text{ to } 10V$
Q_{gs}	Gate-to-Source Charge	--	34	--		
Q_{gd}	Gate-to-Drain (Miller) Charge	--	40	--		

Resistive Switching Characteristics Essentially independent of operating temperature

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
$t_{d(ON)}$	Turn-on Delay Time	--	51	--	ns	$V_{DD}=50V, I_D=50A, V_{GS}=10V, R_G=6\Omega$
t_{rise}	Rise Time	--	75	--		
$t_{d(OFF)}$	Turn-Off Delay Time	--	94	--		
t_{fall}	Fall Time	--	28	--		

Source-Drain Body Diode Characteristics $T_J = 25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions
V_{SD}	Diode Forward Voltage	--	--	1.2	V	$I_S=50A, V_{GS}=0V$
t_{rr}	Reverse recovery time	--	66	--	ns	$I_F=50A, di_F/dt=100A/\mu s$
Q_{rr}	Reverse recovery charge	--	115	--	nC	

Typical Characteristics

Fig.1 Typ. transfer characteristics

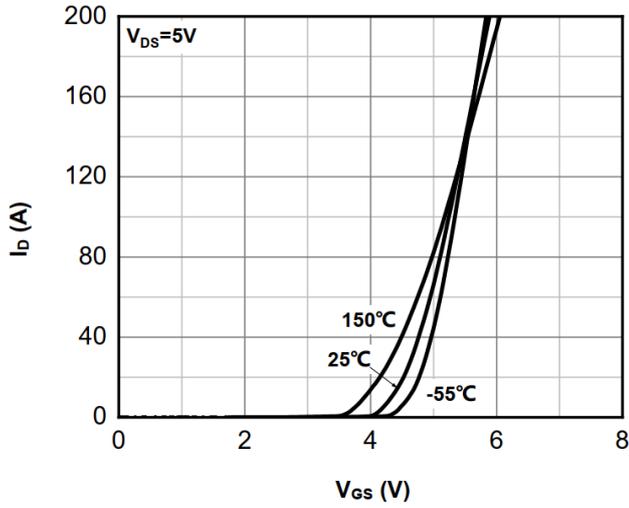


Fig.2 Typ. output characteristics

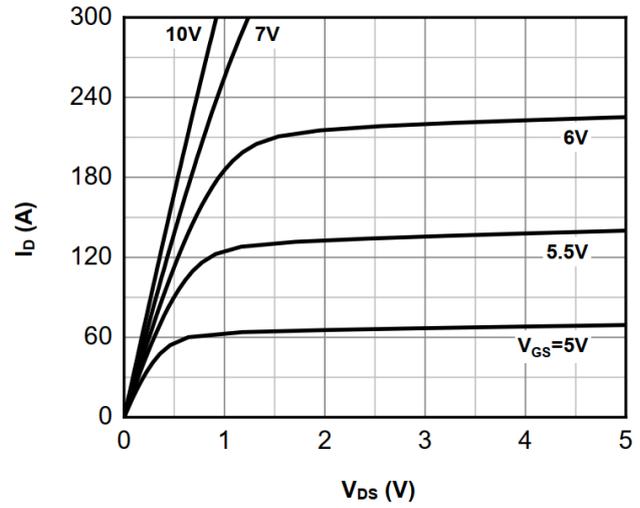


Fig.3 Normalized on-resistance vs drain current

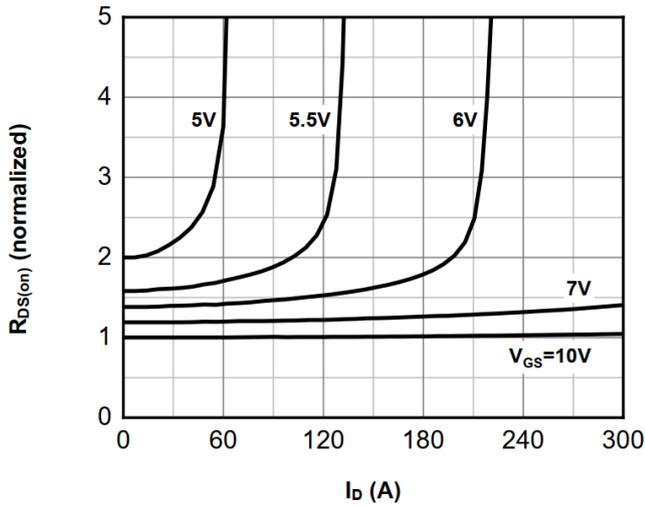


Fig.4 Typ. on-resistance vs gate-source voltage

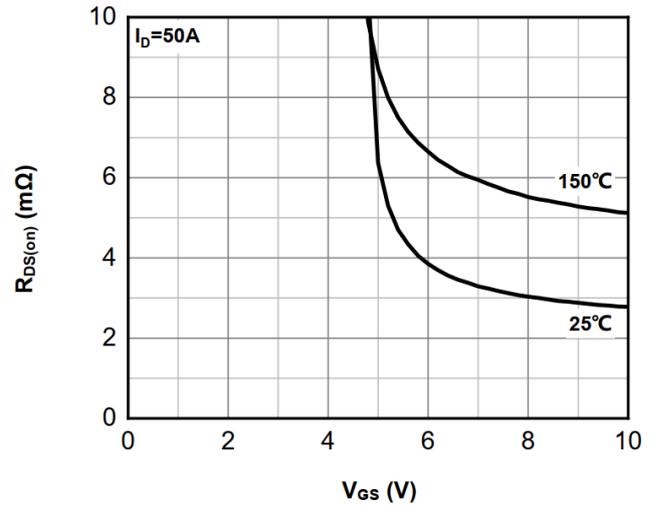


Fig.5 Normalized on-resistance vs junction temperature

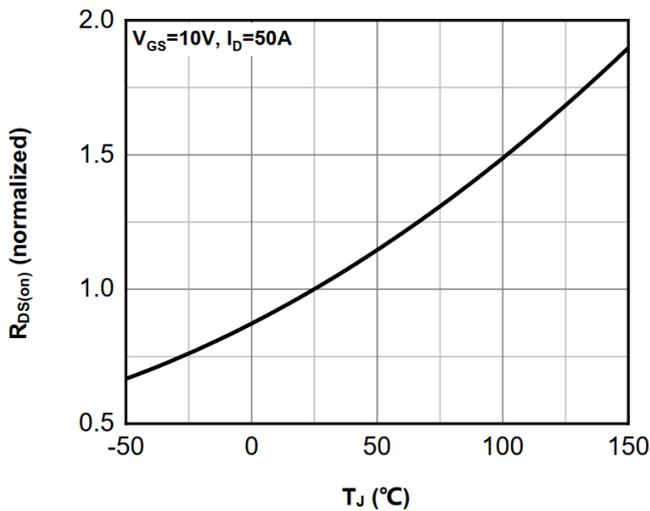


Fig.6 Typ. gate charge

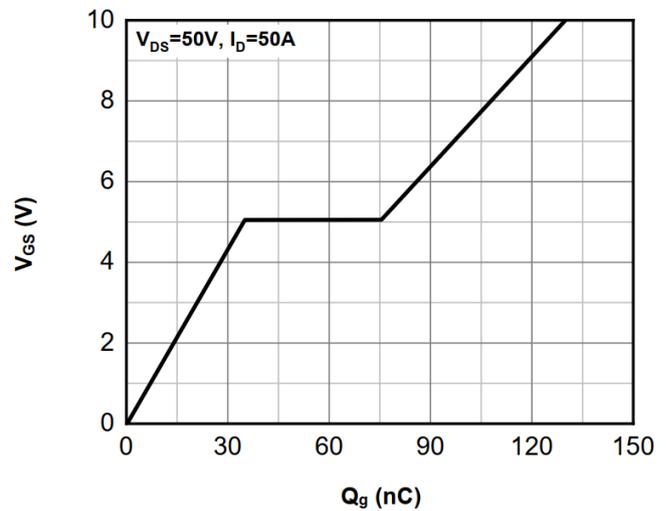


Fig.7 Typ. forward characteristics of body diode

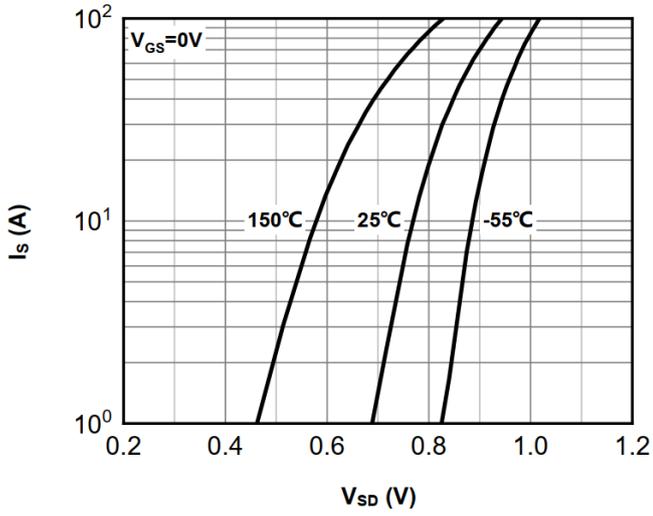


Fig.8 Safe operating area

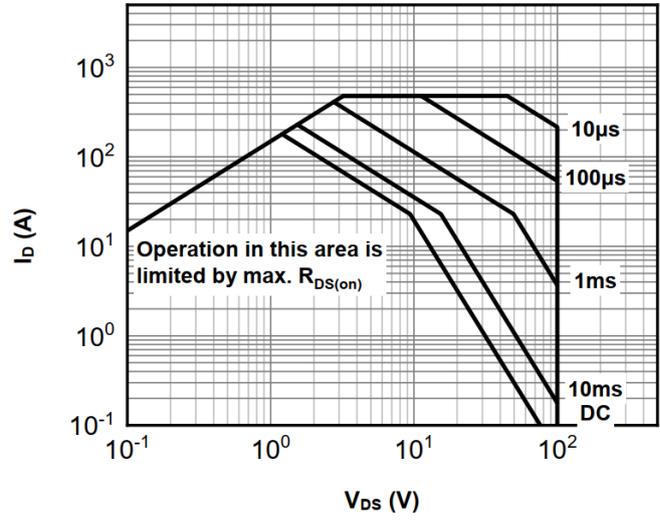


Fig.9 Typ. Capacitance

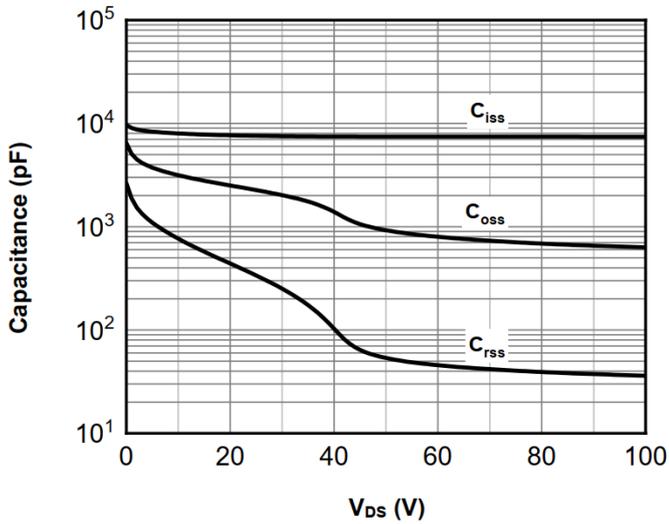
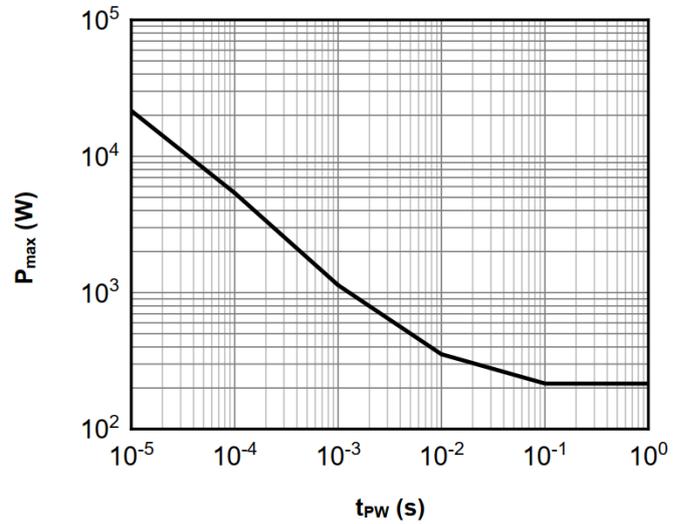


Fig.10 Single pulse maximum power dissipation



Test Circuits and Waveforms

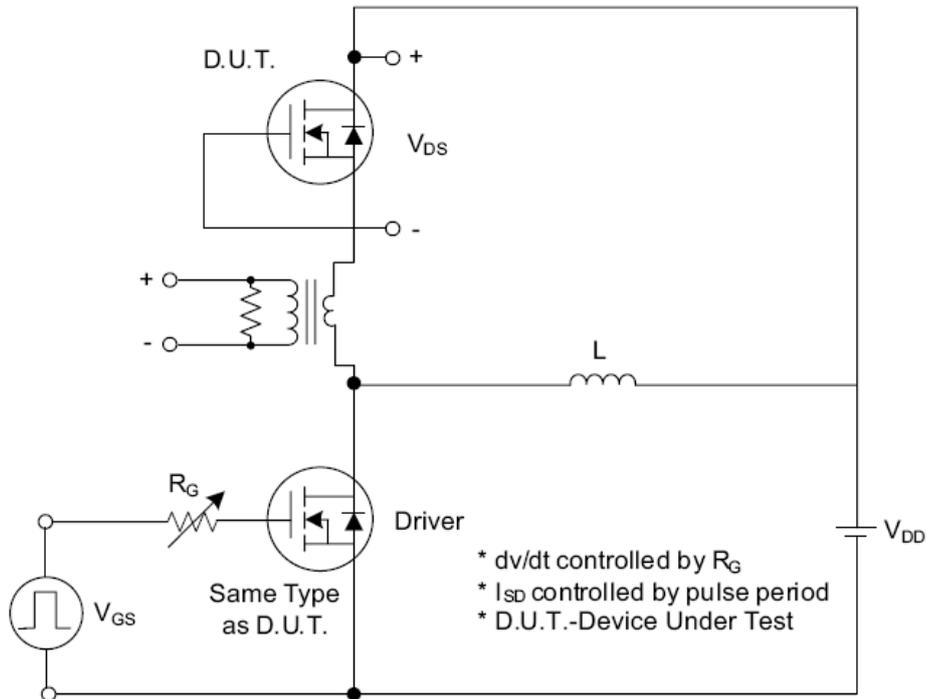


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

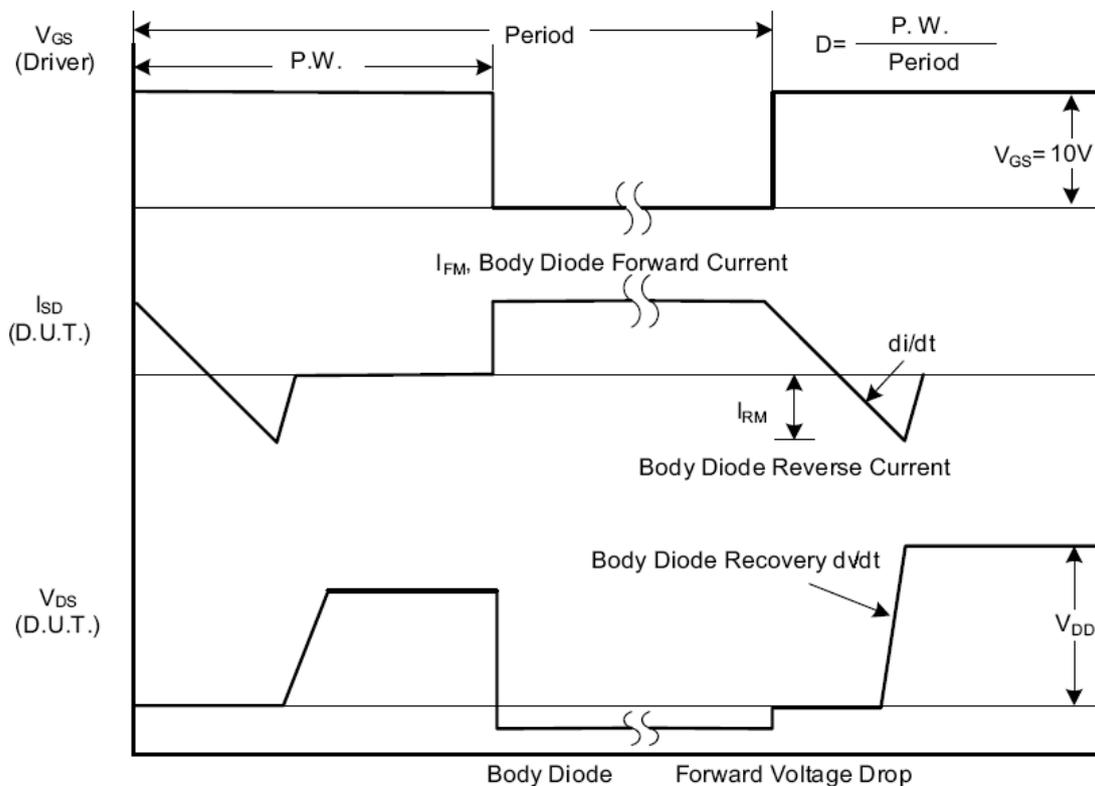


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

Test Circuits and Waveforms (Cont.)

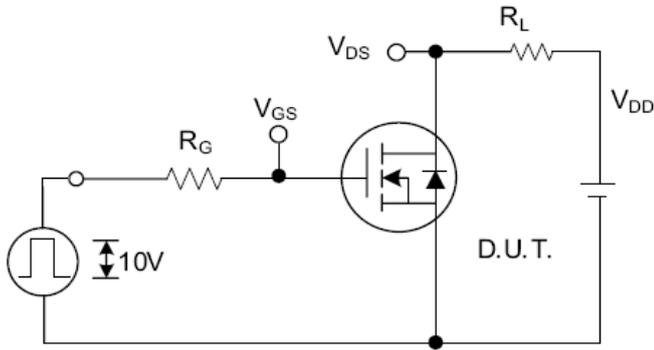


Fig. 2.1 Switching Test Circuit

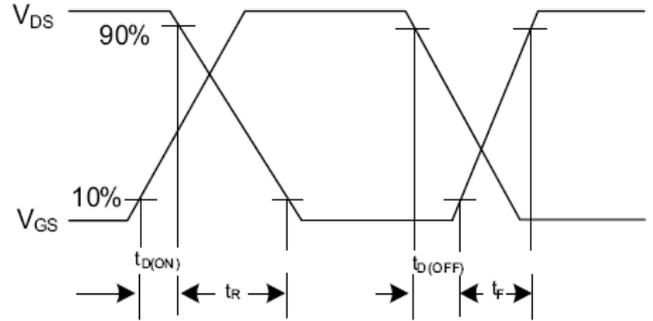


Fig. 2.2 Switching Waveforms

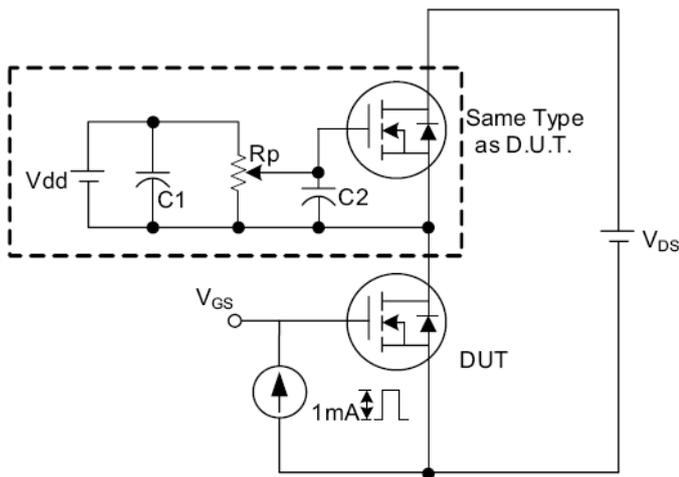


Fig. 3.1 Gate Charge Test Circuit

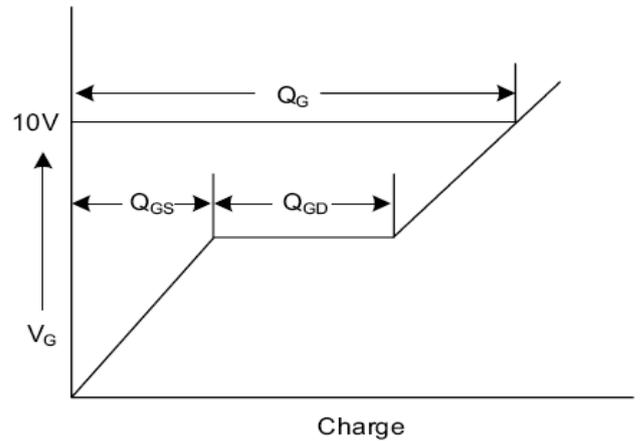


Fig. 3.2 Gate Charge Waveform

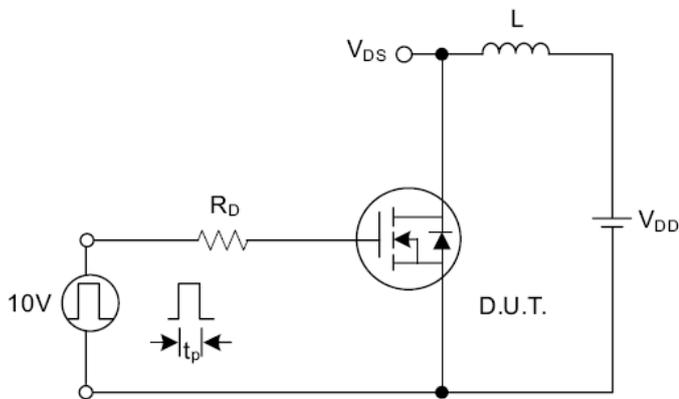


Fig. 4.1 Unclamped Inductive Switching Test Circuit

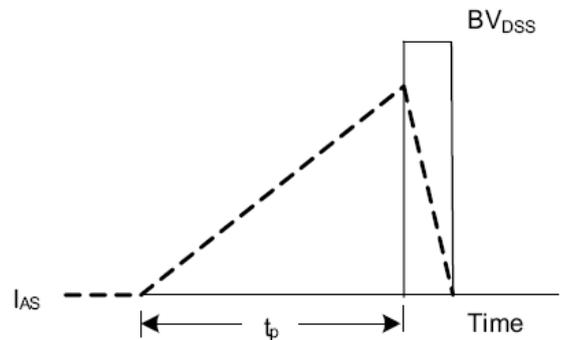


Fig. 4.2 Unclamped Inductive Switching Waveforms

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